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Dear colleagues, dear friends, dear guests,

The 6th SSSS Conference is continuing the tradition established in the year 2000 when the First Small Systems Simulation Symposium took place, here, in the city of Niš at the Faculty of Electronic Engineering of the University of Niš. And now after 16 years one could ask what the frequency of our gathering is? How it happened that in 16 years we have six meetings? The "secret" is very simple. First three Symposia were occurred with time step of five years. Then after 2010, on the request of scientific community, we decided to meet more often - each two years.

The idea about gathering to "promote our research results and especially the results of our young associates in an environment and atmosphere that was supposed to be correctly critical and, in the same time, encouraging enough for further endeavours" come from Prof. Vančo Litovski. He has established SSSS and I want to express my gratitude for this heritage. At the beginning it was not easy to attract scientists from abroad to participate to a new Symposium. However Prof. Litovski has asked his friends from the University of Southampton, Middlesex University, University from Besancon, Technical University of Vienna, Deft University, and others to send papers and SSSS2000 was born as an international meeting. Later on, support from Balkan countries was priceless, as well. Our colleagues from Belgrade, Banja Luka, Sarajevo, Novi Sad, Skopje, and Sofia become our regular participants. This has helped to rebuild some old connection and to establish some new. Moreover, we had participants from Spain, Germany, Armenia, and Australia. In a friendly atmosphere new ideas have emerged so that SSSS participants have appeared as consortia in few European projects.

This friendship was established on professional respect and consequently it lasts ever since. We are gathered again to present results of our bi-annual efforts not just to promote our achievements but also to introduce the young associates in this community.

The keyword of SSSS points to simulation. Simulations appear here in all their shapes and forms: starting from modelling and simulation algorithms ending as a tool for design verification.

This year we have papers categorized in two sessions dedicated to modelling and two to simulations. We cover everything from modelling arks and 3D Tesla´s generator/motor, over modelling effects in FinFETs, telecommunication and information networks, to the modelling electrical vehicles. In simulation area there will be papers about simulators, new implemented simulation methods, and simulation results on system and circuit level.

Special plenary session will be dedicated to the bottle-neck of our scholar system – cooperation between academia and SMEs. We are going to see presentations from Professor Simon La Blond from the University of Bath, the leading UK university with an international reputation for teaching and research excellence, and the Rector of the Metropolitan University from Belgrade, Professor Dragan Domazet about their experiences in this area.

This Symposium would not happen without broad support from Faculty of Electronic Engineering, all members of LEDA laboratory and especially Dr Marko Dimitrijević, as well as from the Innovation Centre of Advanced Technologies, from Niš and particularly Dr Jelena Milojković.

Respectfully
Prof. Predrag Petković

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A Mechanism for Collaboration Between Industry and Academia in the UK, Exemplified by Project SYNAPS

Simon Le Blond and Vančo Litovski

Invited paper

Abstract – Whilst often working in separate silos, there are huge rewards in effective collaboration between industry and academia. Complex modern engineering challenges also necessitate working within a team of teams – *meta-team-working*. We exemplify how academic and industrial collaboration combined with *meta-team-working* may be leveraged through the Innovate UK Energy Catalyst funding mechanism, specifically project SYNAPS, a technically challenging project focussed with smart low-voltage power distribution networks with a heavy simulation component.

Keywords – Research funding, collaboration, power network simulation.

I. Introduction

Within the engineering world, the path of least resistance is for industry and academia to operate in very separate silos. Often this is down to conflicting goals: the key performance metric for academic career progression is to disseminate new knowledge through publication, whereas industry must protect and monetise intellectual property. For these reasons among others, academics and industrialists can have very different mind-sets, attitudes and beliefs that can make collaboration problematic.

However, there are potentially huge rewards from close collaboration. Deep specific, fundamental and focussed knowledge in a particular field can be transferred, applied and commercialised through the right partnership. Moreover specialist *real world* knowledge, for example that which is commercial and regulatory as well as technical can inform and direct fundamental research. So the best functioning partnerships therefore become mutually beneficial and symbiotic.

It is a truism to say that well into the twenty first century much of the easy advances - the *low hanging fruit,* in science and engineering has already been picked. One just has to look at increasing trend in numbers of authors on scientific publications to conclude that even incremental breakthroughs require large collaborations of many researchers from a range of disciplines. A recent paper from CERN regarding the Higgs Boson set the record at over 5000 authors [1]! In the information age, our complex modern world relies as much on the division of expert knowledge as the production lines that drove the industrial revolution relied on the division of labour. Complex modern engineering problems often require *Big Engineering.* This is the harmonious, channelled application of knowledge and expertise from a number of specialist entities to achieve a specific outcome or set of interrelated outcomes. This structured meta-team working is contrary to the pressure to appoint and retain "research stars" in academia; well known personalities that give kudos to an institution, helping to accrete funding and students. However it is also true that the contribution from one particular individual can far outstrip the combined contributions of many, particularly in innovation: a study [2] concluded there was an approximate variation in productivity in programmers of 20:1. Going further, Bill Gates is, (perhaps apocryphally) accredited for asserting "A great lathe operator commands several times the wage of an average lathe operator, but a great writer of software code is worth 10,000 times the price of an average software writer." So star individuals can play a role in providing a step change if they are lucky enough to occupy the tail end of the Boltzmann-like distribution of ability: they achieve the escape velocity necessary in the way that the combined efforts of others will not.

In academia the analogy can be thought of like a theatre *company* where the stars are equally important, if not more so, than those doing the directing and producing. In this paradigm those off stage cannot necessarily do the job of the actors, in the same way that a research manager may not have the expertise to conduct the work of the researchers (s)he is supervising. In engineering industry the structure is much more hierarchical such that those at higher levels normally have the skills and knowledge to do the work of those below them. They are therefore given greater responsibility (and remuneration) and solve complex outcomes through divide and conquer – breaking up small parts of the problem onto complex Gantt charts and allocating the human resource appropriately. Since there are advantages to both paradigms, their hybridisation when academia and industry meet can be very effective and also lead to better understanding and new ways of operating for both parties. For the very same reasons, these two world views can lead to tensions particularly between researchers and industry executives who at first have little mutual empathy due a lack of understanding about the pressures they face.

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This paper presents a high level discussion of the Innovate UK / EPRSC mechanism for collaboration in the hope that it will provide a useful template at various levels of scale for those faced with catalysing a functional symbiosis between industry and academia.

The SYNAPS (Synchronous Analysis and Protection System) project is an Energy Catalyst Mid-Stage Innovate UK/EPSRC project aiming to developing smart grid technologies to the low voltage power distribution network. Within SYNAPS the authors are responsible for delivering a work package with a heavy power system simulation component. We use the SYNAPS project to exemplify how academic-industrial collaboration may be orchestrated. In particular we examine the key players in the UK power industry, those at the vanguard of the smart grid, both external and within the consortium and how good working relationships can be forged amongst these entities.

The rest of the paper is organised as follows. In section 2 we discuss the general funding ecosystem going into more detail over SYNAPS funders, Innovate UK and EPSRC. In section 3 we examine the UK power industry. In section 4 we introduce the SYNAPS project with a brief technical overview, and in section 5 discuss how collaboration inside and outside can achieve the ambitious technical goals by meta-teamwork. Finally we draw some general conclusions.

II. UK Research Funding Ecosystem

A. General Overview

In the UK, funding for research innovation comes from many sources, although this section is written from the perspective of the authors, academics in electronic and electrical engineering. With this in mind, our main funding sources are:

- Research Councils UK [3]:

An umbrella organisation for 7 broad discipline focussed UK academic research councils, with those particularly relevant to electrical engineering being EPSRC, (Engineering and Physical Sciences Research Council) NERC (National Environment Research Council and STFC (Science and Technology Facilities Research Council). These bodies use specifically scoped calls alongside standard "responsive mode" with open scope, both awarded through a rigorous peer review process, usually including a panel stage.

- European Research Council (ERC) [4]:

European Union Funding, currently migrating from Framework Programme 7 to Horizon 2020 [reference website]. European funding rules often necessitate consortia of many partners both academic and industrial across at least 3 EU countries so rely on large critical mass to be viable.

- Direct Funding from the UK Government:

Various government departments may commission targeted research calls.

- Innovate UK [5]:

An executive non-departmental public body sponsored by the government department for Skills Business and Innovation set up to de-risk research and development.

- Collaborations with various partner research councils across the globe, usually focussing on mobility and seed funding.
- Finally an industrial partner may outsource research to an academic institution if they are unable to undertake it internally.

With the exception of the international and private sources, the UK Government pays into these expert bodies to distribute money as they see most appropriate, so in some sense, the UK Tax Payer is the ultimate source of most research funding. Clearly public money must be used responsibly and thus the research from these areas is subject to the highest levels of scrutiny: both auditing, monitoring and reporting throughout the grant lifecycle to ensure the funding is being used effectively.

The particular funder that one targets for a grant proposal is highly dependent on the type of work, the research outcomes and the parties required to achieve these, in addition to the stage of career of the principal investigator. A pure research project in engineering may be most directly suited to EPSRC funding, whilst one closer to commercial application would be more relevant to either Innovate UK or ERC. Moreover it is unlikely that grant reviewers will entrust large sums of money to early stage career researchers without an established track record, regardless of the merit in their idea.

B. EPSRC

EPRSC (Engineering and Physical Sciences Research Council) is the UK's main agency for funding research in engineering and the physical sciences, investing up to £800M p.a. in research and postgraduate training [6]. It is the primary source of funding for pure physical sciences research more blue sky "engineering research" and is thus the first stop for academics who wish to fund a research project confined within their own institution or with one or more academic partner institutions. EPSRC's strategic plan [7] informs on "grow" "maintain" and "reduce" subject areas within the portfolio and thus the case for supporting a particular grant can be enhanced if it aligns with EPSRC's overall strategy.

C. Innovate UK

According to their Website, Innovate UK is "the UK's Innovation Agency" [5]. Their remit is to

- determine which science and technology developments will drive future economic growth.
- meet UK innovators with great ideas in the fields Innovate UK are focused on.
- fund the strongest opportunities.
- connect innovators with the right partners they

need to succeed.

- help innovators launch, build and grow successful businesses.

D. Energy Catalyst

Energy globally is regarded as a major societal challenge – the compounding problems of climate change, limited fuel resources (and their increasingly uncertain supply chains) increasing population, global industrialization and the accompanying load growth combine to form an "energy crisis" that is one of the greatest existential threats to human civilization. On the other hand, the UK government recognizes that there is huge global commercial opportunity for UK plc in meeting this challenge.

The Energy Catalyst is a rolling funding scheme overseen by Innovate UK to support technology projects addressing all three corners the "Energy Trilemma": the competing need to reduce emissions, improve security of supply and reduce costs (see Fig .1.) There are three tiers of funding awards: early stage, mid stage and late stage with funding capped at £300 K for early feasibility studies, £3 M for mid-stage technology development and £10 M for pre-commercial technology validation respectively. Mid stage and late stage must be business led and collaborative but may involve academic partners or any other research organisation who are permitted to absorb up to 30% of total project allocation. Crucially, the funding for academic partners comes from EPSRC and is funded at 80% Full Economic Costs (which in the author's world is synonymous with "fully funded" due to the complex array of overheads that RCUK are willing to fund and those that they are not). Innovate UK defines the separate players in this ecosystem as 1. Research institution, 2. Small/micro SME (Small Medium Enterprise) 3. Medium SME and 4. Large Business. This demarcation points are summarized in table 1 which also shows the level of match-funding that each entity must contribute themselves.

It is worth explicitly noting, with reference to table 1, that with these carefully graded funding rules, the industrial partner must match fund a portion of their own project costs with a higher percentage investment the closer they are to commercial readiness, such as to drive the eventual commercial exploitation of the project IP. Also, since the research institution is not expected to commercialise their IP they are not asked to risk the match funding. The negotiation of Collaboration Agreements between all partners is necessarily complicated as it must allow for the free flow of information between the partners to collaborate in the project, but also simultaneously protect the commercial interests of the industrial partners and the academic partner's remit to disseminate research outcomes. Innovate UK therefore supplies a template Collaboration Agreement to assist SMEs that may not have access to, or the resource, to outsource legal assistance. In addition it is vital all partners must be under NDA (Non-Disclosure Agreement) in order to even begin working on the proposal, let alone the project itself. Despite these safeguards, all partners, particularly the SMEs are exposed to a high level of commercial risk through leaked IP, whether by design or by accident. It is therefore imperative that partners behave with impeccable business ethics and build up mutual trust at the consortium building stage before embarking on a project.

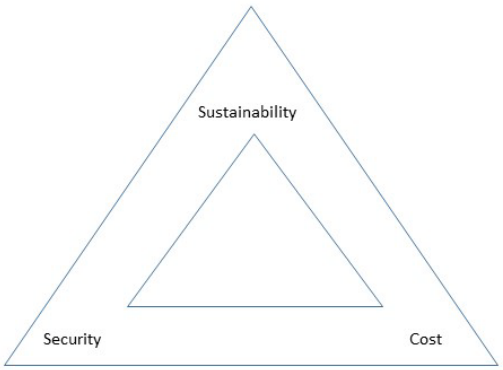

Fig. 1. The "energy trilemma" illustrating the competing needs in the energy crisis to reduce emissions, improve security of supply and reduce costs. It is very difficult to meet one or two of these without compromising heavily on the third.

III. UK Power Industry

Before discussing Project SYNAPS it is necessary to briefly summarise the UK Electrical Power Industry. The UK power industry was globally one of the first utilities to be privatised in 1990. Since then, the national transmission grid, the supply side and the regional distribution networks have all been operated and owned by private entities.

TABLE I
Energy Catalyst Funding Tiers

Scheme	Total funding available	Research Institution	Small SME <50 people, turnover £10 M	Medium SME < 250 people, turnover £50 M	Business
Early Stage	£300 k	80% FEC <50% total project cost	70%	60%	50 %
Mid Stage	£3 M	80% FEC <30% total project cost	70%	60%	50 %
Late Stage	£10 M	80% FEC <30% total project cost	45%	35%	25 %

The UK government recognizes that the overseers of generation, transmission and distribution necessarily hold natural monopolies and thus appoints a regulator - *Ofgem* - to protect consumers. Businesses can be liable for heavy financial penalties for any breach of contract or exploiting their monopoly.

Suppliers or retailers are companies that purchase electricity on the wholesale markets from generators and then sell it to customers – commerce, industry and domestic alike. Most UK consumers have a vague notion that retailers are those responsible for getting electricity to their power sockets. However this role is fulfilled at a national level by National Grid, the Transmission System Operator (TSO) and then at a regional level by the eight Distribution Network Operators DNOs, who are collectively responsible for the operation and maintenance of the electrical power network infrastructure. Electrons are not so discerning of these arbitrary boundaries so power flows at light speed down wires using alternating current at a system-wide nominal frequency of 50 Hz. The High Voltage Transmission Network and can be thought of the highways whilst the distribution network at lower voltages are the trunk roads all the way down to individual driveways. There is presently a trend towards decentralization of energy infrastructure to better facilitate low carbon economy. Historically, the system was designed around large centralized thermal based power plant. Many cleaner energy sources and energy storage technologies suit connection at lower voltage levels and therefore the distribution networks are becoming more active with bi-directional power flows, with micro-generators selling their power back to the grid as well as consuming it. Contrary to this drive, ageing infrastructure is being pushed well beyond its expected lifetime leading to a huge asset management problem, particularly within the oldest parts of the network: the low voltage (LV) distribution network. This puts two fold pressure on the LV voltage network – the requirement to modernize the aging assets and the requirement to modernize into a "smart grid" to accommodate connection of new energy technologies. This also creates a massive business opportunity in LV networks.

IV. Project SYNAPS – Technical Overview

Project SYNAPS (SYNchronous Analysis and Protection System) is a £1.7 M Innovate UK energy catalyst mid-stage project currently underway, addressing the problem of LV network modernisation directly by developing an array of inter-related Smart Grid LV network technologies. In this section we will give an overview of its technical themes.

A. Higher network visibility

Essentially the core SYNAPS technology will be a way of monitoring network conditions at extremely high granularity. This involves measuring the physical quantities of voltage and current waveforms in the 415 V three phase network at high sample rates (~200 kHz) and then inferring knowledge about the network in real time or near real time. This unlocks a whole host of new functionality. For example, a big issue for network operators is knowing the topology of the LV network itself. Like capillary level blood vessels in the human body, the LV network is vast and sprawling and often "multiply patched" since over time it has grown sub-optimally and organically, following the incremental growth of the built environment. DNOs therefore often have poor historical records of exactly what assets they have at LV. SYNAPS will develop a monitoring platform able to infer network topology.

B. Pro-active Maintenance

A particular problem is progressive water ingress into cable insulation causing arcing short circuit faults. This often initially causes an intermittent fault that does not always melt the protective fuse but nonetheless risks damage to connected equipment. The DNO only has knowledge about this problem when the fuse eventually does operate, and customers call in to complain they have lost supply. The DNO responds by physically sending maintenance personnel out to replace the fuse. If the fault persists the fuse will then operate again necessitating digging the cable up and replacing it. This cumbersome process leads to many customer minutes off supply and large financial penalties to the DNO from the regulator. SYNAPS will be able to use pattern recognition techniques to detect early when an intermittent fault will occur and thus maintenance can be proactively organised to avoid customer minutes lost.

B. Protection and reconfiguration

The protective fuse is itself a very crude device. It only operates once before requiring replacement and its operating characteristic is limited to an inverse time-overcurrent. At higher voltage levels the network is protected by circuit breakers that use sophisticated fast digital relaying algorithms to operate in milliseconds following a fault, overseen by carefully coordinated settings of the overall protection system. This approach keeps as much of the healthy system live whilst isolating the faulted part. SYNAPS will apply this paradigm to the LV network.

With a partially meshed or fully meshed network, there is the possibility of routing power from a different source and thus bringing customers back on supply before a permanent fault can be fixed. There are complex safety and technical implications that must be considered before doing this. With regard to the technical, low carbon stresses such as micro generation and electric vehicles will make the situation more complex: for example if they remain connected under faults they can potentially create an

unintentional islanded network. SYNAPS will consider these aspects and develop new reconfiguration algorithms for the LV network.

C. Solid state switchgear

An important gateway technology at LV would thus be replacement for the fuse: a switch that can be tele-operated and that can interrupt heavy short circuit currents that arise under fault conditions. SYNAPS is thus researching and developing solid-state switchgear than can operate much faster than electromechanical devices by using power electronics. Regardless of the final choice of technology, the ability to tele-operate SYNAPS switchgear will unlock much more sophisticated protection and reconfiguration algorithms.

D. Network Simulation

Real world fault data on actual systems is scarce because these systems are not monitored and live tests are expensive, disruptive and dangerous. Therefore in achieving the SYNAPS outcomes there is an overarching requirement to simulate various fault scenarios in the LV network in high levels of detail. The authors are thus tasked with time domain simulation of various LV network topologies. In the first stage this involves simulating fault waveforms "offline" with tools such as SPICE and ATP-draw (the modern graphical version of EMTP) to conduct electromagnetic transient simulation, to create waveform data that can be fed into to machine learning inference engines. In the second stage the simulations must be in real time such that the developed SYNAPS platform can be tested and validated.

The RTDS is a power network simulation hardware tool that allows any power system to be digitally simulated in real time at a base time step of 50 μs, confined only by the amount of modular processing power available [8]. See figure (2). The RTDS has the very powerful feature of putting hardware into a closed loop in the simulation through various I/O ports. In more detail the RTDS can simulate the power system, synthesising real voltages and currents as they vary with time using digital to analogue conversion and then send these signals to outboard equipment – in this case, the SYNAPS platform. The SYNAPS equipment can do the required processing and then send analogue or digital signals back to the RTDS, automating network tasks. This could be opening or closing a switch following a fault, for example. Due to the aforementioned difficulties in real world testing, this step is a vital test and validation task before utilities are comfortable deploying SYNAPS on a real power network.

An interesting technical challenge in SYNAPS is digitally simulating the electrical fault arc – the high channel of ionised plasma when an insulating medium breaks down - which is a complex physical phenomenon [9]. This involves computing the time varying arc conductance in every timestep using differential equations. Interested parties are referred to the paper in the SSSS conference proceedings by the same authors confined to this very subject that develops a new model specifically for arcs propagating through cable insulation [10].

V. Project SYNAPS – The Consortium

A technically ambitious and complex project such as SYNAPS requires an array of various specialisms to be channelled and focussed into a concerted harmonious

Fig. 2. The RTDS (Real Time Digital Simulator) allows real time simulation of Power networks and can connect hardware in the loop.

effort. This is a kind of *meta-teamwork* in as much as it requires a team of teams. Within the consortium we therefore have assembled three companies, classified under Innovate UK as micro-SMEs, and two partner universities. In addition a large established micro-processor manufacturer is offering contribution in kind with chip development platforms in line with a strategic view onto the smart grid market.

The industrial project partners are:

- Power Line Technologies (Project leaders)

PLT designs, manufactures and markets solutions in the smart grid and communications market place. The Company has expertise in LV & MV smart grid, telecommunications, powerline communications and network management. It has already established relationships with distribution and transmission network operators for its solutions.

- Akya Ltd

Akya Ltd are responsible for developing the chips that will process the SYNAPS data. Akya specialises in the

development of advanced bespoke digital signal processing solutions for high performance and / or low power devices. Akya's ART technology is capable of providing highly-optimised, application-specific, fully programmable DSP cores with a power/performance far better than that which can be achieved by conventional general-purpose DSP designs.

- Techna Ltd

Techna are producing the SYNAPS LV switch gear. With over seventy years of electrical engineering experience Techna are specialists in advanced circuit protection products.

The academic partners are:

- University College London (Department of Mathematics and Statistics) are developing the machine learning algorithms that will take LV network data and infer information about the network.
- University of Bath, Centre for Sustainable Power Distribution (CSPD) is contributing its expertise in real time digital simulation and transient based protection to generate fault data to validate the SYNAPS platform. (The authors of are from the University of Bath.)

Since SYNAPS is a truly collaborative project, there is necessarily much interdependency between the partner work packages. For example it is important that the simulation data is supplied on time, and that developed software algorithms can be delivered in a form to run on the SYNAPS hardware. All deliverables are therefore synched to a common time grid of quarterly milestones over the 2 year project lifespan.

It is also vital therefore to establish good working relationships, clear channels of communication and regular reporting between the partners. In addition due to the modest size of the industrial partners, many of those involved must fulfil both a high level executive role and a detailed technical engineering role.

Formal project meetings may therefore become too large and unwieldy for detailed intimate technical discussions that concern only two or three partners. Therefore to facilitate cross-partner technical work there are three technical coordination groups (TCGs) with a different focus and combination of membership of the relevant project partners. The TCGS favour small and agile working between technical personnel (or those fulfilling their technical role) within different partner entities. To facilitate this inter-partner collaborative working various web based software tools are invaluable. For example Skype is ubiquitous free software for VoIP conference calls. However Cisco's WebEx also allows screen sharing and meeting recording across multiple remote guests and user. The Confluence software by Atlassian allows a web based focal project repository of documents, media and meeting minutes to be shared and edited collaboratively. However none of these can currently replace the nuances of a physical face to face meeting, so often it is necessary to travel and it is important partners distribute the burden of travel and hosting fairly across the consortium. All other things being equal, it is perhaps therefore better to choose partners that is within a reasonable distance. Face to face meetings are a great opportunity to conduct partner site visits and socialise (with the help of appropriate choice food and beverage of course to lubricate and celebrate progress).

SYNAPS brings together engineers from different disciplines that have a slightly different technical vocabulary. Computer science (hardware and software), electronics engineers, mathematicians and electrical engineers have a lot of overlapping knowledge but the Venn intersection clearly does not cover the specialist knowledge within each discipline. (If it did there would be no added value in *meta-team work*…) It is therefore vital that the partners have empathy for different levels of technical knowledge and understanding within the consortium, and tread the fine line between informing and condescension when explaining concepts to non-expert-colleagues. However this is also a great opportunity, not just acquiring complementary knowledge from a different discipline but also enhancing understanding of one's own. In academia the symbiosis between the pillars of teaching and research is mutually reinforcing because being able to teach and explain a high level concept necessities the highest form of understanding in the teacher. Like students, colleagues from different disciplines can often ask uncomfortable fundamental questions that can helpfully critique an idea for feasibility and robustness; a question that might not occur to an expert peer in the same area due to mutual assumed knowledge.

In order to succeed the SYNAPS consortium must interface with various external power industry organisations. In particular, close working with DNOs (Distribution Network Operators) is necessary to acquire technical data and also scope market requirements since the DNOs will be the main customers of any commercial offering. Here too empathy and emotional intelligence is required. Utilities have a huge challenge maintaining and operating the network within regulatory limits with limited human technical and financial resources. Therefore in acting responsibly they are understandably wary of any new technology due associated risk and large learning curve. This results in an extremely conservative industry, where simple elegant design is preferred over feature laden sophistication. Whilst power systems technology may appear to evolve at a glacial pace to engineers with an ICT background, it is important to remember the utilities must maintain a complex interconnected system with 100% reliability and safety. The consequences of a smart phone widget failing are rather less drastic than a transformer protection relay failure. One leads to an angry customer review whilst the other leads to a substation explosion, customers without power and potential loss of life. The DNOs have unequalled intimate knowledge of the

interrelatedness of their networks and the resulting design philosophy which should be respected all costs. It is therefore necessary for SYNAPS to engage with utilities early establishing rapport for functional partnerships founded on mutual respect and empathy. This of course extends to any technology project where the end users are not within the consortium: regular engagement with the customers from the start is vital.

CONCLUSION

This paper has discussed the merits of collaboration between academia and industry and coined a new expression *meta-team-working* – working in a team of teams. Interdisciplinary *meta-team-working* is needed to solve complex modern engineering challenges. For successful *meta-team-working* the ways of operating, cultures and vocabulary must be respected and understood. The very same challenges also bring great opportunity for widening the horizons for all those involved.

We have exemplified this thesis though the innovation funding ecosystem in the UK and in particular the Innovate UK Energy Catalyst project SYNAPS which is developing smart grid technology in LV power networks. Here as with all such projects there is need for effective communication, empathy and mutual respect, in all directions within the organisational model.

ACKNOWLEDGEMENT

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[10] Our paper?

Co-operative Education Programs with IT Companies at Belgrade Metropolitan University

Dragan Domazet

Abstract - In this paper a description of the cooperative educational program of Belgrade Metropolitan University is described. It implements a parallel co-op model as students simultaneously follow regular courses and work. The BMU Co-op model provides students with paid tuition fees, scholarships and the prospect of a job after graduation. An IT company also has many gains by providing these benefits to students. It can employ a group of graduated IT students each year, specially educated for the company, as these graduated students, its scholars, have four years of work experience in the given company during their studies.

Keywords – Cooperative education, education of IT and software engineering students, internship

I. Introduction

IT companies these days often have difficulties to recruit new engineers with needed knowledge and skill sets. The demand is high and the offer of fresh graduated students is not sufficient and furthermore, in many cases not in line with requirements of employers. Due to the high demand of IT engineers, many students start working even before completing their studies. This may have a negative impact to their professional development. On the other hand, companies need to provide additional training to these employed students to solve their short-term problems. However, doing this in many cases creates long-term problems, as these programmers usually never complete their studies and have limitations of their capabilities due to poor and uncompleted education.

Having these challenges in mind, Belgrade Metropolitan University (BMU) has developed a parallel cooperative program for students of its bachelor program in Information Technology, Software Engineering, Game Development and Information Systems. Cooperative educative programs are very popular and developed in Canada [1-4] and USA [5-7], but the cooperative program of BMU has some specific features that will be described in the paper.

II. The Concept of the BMU Co-op Program

A. Periods of Work and Duration

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Cooperative education is a partnership between a university's academic programs and professional employers who provide off-campus work experience. It is a structured way of learning that combines in-class learning with periods of actual work. There are alternating and parallel co-op models. In the alternating co-op model students alternate a semester of academic coursework with an amount of time working, repeating this cycle several times until graduation (Fig. 1.a). The parallel method splits the day between school and work, typically structured to accommodate the student's class schedule (Fig. 2.b). Surveys and analyses [8-11] have reported many benefits for students that cooperation education can provide.

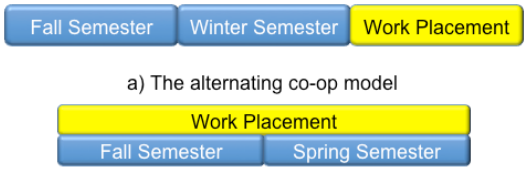


Fig. 1 The alternating and parallel co-op models

The co-operative education program of BMU implements the parallel co-op model. Students follow regular courses having at least 20 in-class hours a week and up to 20 work hours in a company.

During their four-year academic bachelor education, their amount of work in companies is slowly increasing along with their capability to accept more demanding work assignments. During periods of their work, they initially might have more special, short training courses aiming to provide them company-specific know-how (non-formal education), but later they learn more by getting experience in performing their work assignments (informal education), as shown in Fig. 2

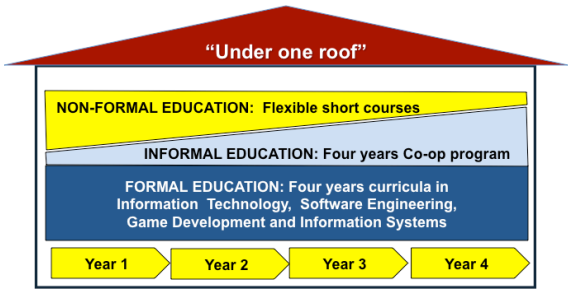


Fig.2 BMU co-operative education model

As students follow academic courses and work simultaneously, it is beneficial if their work placement is as close as possible to the university. At BMU, students study and work in the same building, as its Business and Education Center in Niš (Fig.3) provides the working space to IT companies that participate in the BMU co-op program.

Fig. 3: Business & Education Center of BMU

Having the learning curves of students in mind, BMU co-op programs use different workload distribution of students between academic courses and work terms. Fig.4 shows maximum allowed work of students in a company during a four-year bachelor co-op program. Students may work less, if it is agreed with companies, but not more.

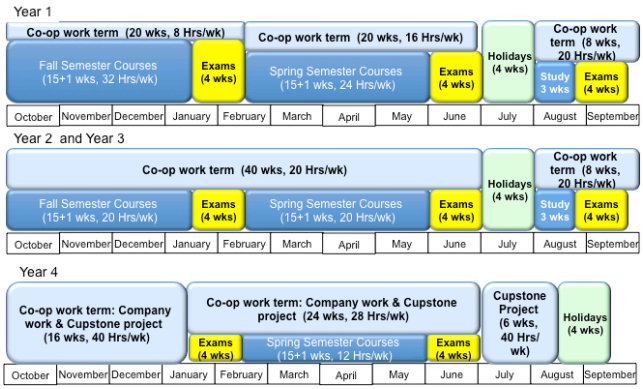


Fig. 4: Workload distribution between work and education for co-op students.

Freshmen students have only 8 hours/week of work in Semester 1 and 16 hours/week in Semester 2. In 2nd and 3rd year, students may work up to 20 hours/week, and in the 4th year they have a full-time work (40 hours/week) in Semester 7 and up to 28 hours/week in Semester 8. The workload distribution of co-op students depends on the company. Table 1 presents two extreme co-op models with a maximum and minimum workload of co-op students during their four years bachelor program. Fig. 5 shows the annual work time of students in case of these two co-op models. Each company decides about its co-op model. The actual co-op model, in most cases, will have the numbers of work hours of students between these two extremes.

Each company can choose the workload model that suites the company best, but it can be between the two extreme workload models given in Table 1 and Fig. 5. It means that the maximum workload is **24 months** and minimum workload is **12 months** during a period of four years (48 months.)

TABLE I
TWO MODELS OF WORKLOAD OF CO-OP STUDENTS

	Model No. 1			**Model No. 2**		
Sem.	Weekly Workload (Hrs/wk)	# of work Hrs/wk	Total # of work hours	Weekly Workload (Hrs/wk)	# of work Hrs/wk	Total # of work hours
1	8	20	160	8	15	120
2	16	20	320	8	15	120
Summer 1	20	8	160	0	0	0
YEAR 1			**640**			**240**
3	20	20	400	16	15	240
4	20	20	400	16	15	240
Summer 2	20	8	160	0	0	0
YEAR 2			**960**			**480**
5	20	20	400	16	15	240
6	20	20	400	16	15	240
Summer 3	20	8	160	0	0	0
YEAR 3			**960**			**480**
7	40	16	640	40	15	600
8	28	24	672	16	15	240
Summer 4	40	6	240	0	0	0
YEAR 4			**1.552**			**840**
TOTAL			**4.112**			**2.040**
	Total work months:		**24,48**	**Total work month**		**12,14**

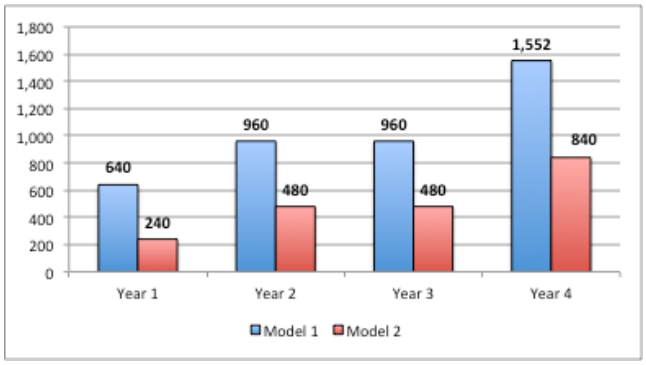


Fig. 5 Maximum and minimum workload of co-op students

BMU co-op partner companies have to provide mentors that work with co-op students and they give them homework and project assignments. Co-op students must submit reports to professors or teaching assistants of each academic course, reporting relevant work they have achieved for each of courses they have in their curriculum.

B. Specifics of the BMU Co-op Education Program

BMU does not require that students find companies (as in Canada, for instance) where they can work during the work terms of the co-op program. BMU makes special arrangement with interested companies and connects students with their companies.

As BMU is a private university and students need to pay tuition fees, it is very important for students to have an option of free education, i.e. to avoid paying tuition fees. Having this in mind, BMU requires that its co-op education business partners pay tuition fees for students that will be their scholars. In return, students have to work in the company during their studies throughout four years, according to the workload model specified by the company and they have to work for the company (if the company asks them) at least four years after the graduation.

It is up to the company to decide the value of their scholarship to be given each month to their scholars during their studies.

For each student, the company, the student and BMU make a contract that specifies the mutual obligations and rights of their participation in the BMU co-op program in detail.

III. Responsibilities of Partners

Each partner has the following responsibilities and obligations:

1. IT Company:
   a. IT Company offers N scholarships to its scholars (for instance, 30, 85 and 250 EUR/month – for 1st, 2nd and 3rd , and 4th year, separately)
   b. IT Company pays tuition fees to BMU: 2.000 EUR per year per student
2. Student:
   a. Partially works for the IT Company and studies
   b. Must acquire 60 ECTS per year with minimum average grade: 8,00
   c. Must work for the IT Company for at least 4 years after graduation.
3. BMU:
   a. Adopts assignments and electives of the scholar to the needs of the IT Company
   b. Provides needed workspace for the IT Company in BEC building in Niš (free 2m^2 per scholar, the rest is rental)

IV. Financial Aspects of the Cooperation

IT companies, not only in Serbia, are facing the problem of lacking of IT engineers and programmers these days. The BMU co-operative education program aims to help solving this problem by:

- educating and developing new fresh IT graduates, based on the contract between the university and the future employer,
- providing parallel work placement of IT students, for at least 12 months during their four years bachelor program.

IT companies, normally, raise few expected questions:

- Are these students useful and can they really contribute to our business before graduation?
- If we have to pay tuition fees for four years, and scholarships to our scholars, is it a cost-effective investment?

The answer to the first question will be provided in next section of this paper, but the answer to the second question is provided here.

Table II shows the cost of a work-hour of a student that is fully covered with the paid tuition fee (2.000 EUR/year) and the scholarship in case of a maximum workload of students (Model 1) and of a minimum workload (Model 2). The level of scholarships depends on the company. Scholarships used in Table II are assumed levels. They depend on students' workload and having in mind that scholarships are not taxed up to 10.600 Din/month (cca 85 EUR/month).

TABLE II
Cost of Students' Work in Case of Two Models of Workload

Model No. 1 (maximum of student work load)

	Total # of work (Hours)	Net Scholarship (EUR/month)	Gross Scholarship (EUR/month)	Gross Annual Scholarship (EUR)	Annual Tuition Fee (EUR)	Cost of student's work (EUR/hr)
YEAR 1	640	30	30	360	2.000	3,69
YEAR 2	960	85	85	1.020	2.000	3,15
YEAR 3	960	85	85	1.020	2.000	3,15
YEAR 4	1.552	250	286	3.436	2.000	3,50
TOTAL	**4.112**			**5.836**	**8.000**	**3,36**
Months:	**24**					

Model No. 2 (minimum work load)

Semester	Total amount of work (Hours)	Net Scholarship (EUR/month)	Gross Scholarship (EUR/month)	Gross Annual Scholarship (EUR)	Annual Tuition Fee (EUR)	Cost of student's work (EUR/hr)
YEAR 1	240	30	30	360	2.000	9,83
YEAR 2	480	85	85	1.020	2.000	6,29
YEAR 3	480	85	85	1.020	2.000	6,29
YEAR 4	840	250	286	3.436	2.000	6,47
TOTAL	**2.040**			**5.836**	**8.000**	**6,78**
Months:	**12**					

If a company implements the assumed levels of scholarships, in case of the maximum workload of students (Model 1), the average cost of students' work is **3,36 EUR/hour** (both scholarship and tuition fees are included). In case of a minimum workload of students (Model 2), the average cost is **6,78 EUR/month**.

Table III gives a comparisons of these costs with the cost of work of a junior programmer, employed full-time, having an assumed starting net monthly salary of 600 EUR/month Table III shows that the cost of work of

students during their studies (3,36-6,78 EUR/hour) is lower or comparable with the cost of work of a junior programmer (6,42 EUR/month or more). It means the BMU co-op program offers to IT companies a cost-effective investment in the education of their future IT engineers. If a company has projects and work assignments for its scholars, they can pay-off all investment to their education (tuition fees and scholarships). As IT companies charge the work of junior programmers much more than the cost of work of its scholars, it is realistic to expect that the work of its scholars during their studies even creates some profit to the company.

TABLE III
COST OF STUDENTS' WORK IN CASE OF TWO MODELS OF WORKLOAD

	Model of Work placement with equiv. 1.840 Hrs/yr	Gross Cost per Hour (EUR)	Assumptions
1	Co-op model 1	3,36	if student works 1.840 hrs/yr
2	Co-op model 2	6,78	if student works 1.840 hrs/yr
3	Junior programer	6,42	for nett salary 600 EUR/mnt

It is fair to mention that in this analysis some cost factors are not included, such as:

- Cost of mentoring of scholars
- Cost of special training courses of scholars
- Cost of learning time of scholars, when they do not work, but learn what they need to know for a task to be assigned to them.

Having the market cost of work of junior programmers in mind, all these cost factors cannot change the general conclusion that the company can earn enough to recover its investment to its scholars, by using them in its projects during their studies. The costs factors given above are usual cost factors that companies have when employing new graduated IT engineers. So, these cost factors are not specific to the co-op program. In case of the co-op program, this cost incurs earlier than normal (when graduated engineers start working for the company).

The cost-effectiveness of a co-op program, that is obviously achievable, is not most important for IT companies. The most important result of the implementation of co-op programs for IT companies is *the solution of the problem of recruiting new IT engineers.* By implementing the proposed co-op program, a company may employ a group of new graduated IT engineers, its former scholars, each year. These engineers are fully effective from the first working day, as they are familiar with the technology and work standards of the company, as they were involved in its projects in previous four years, during their studies.

V. CAN STUDENTS DELIVER WHAT IS EXPECTED?

It is normal to raise this question, when someone has to decide whether to invest in students' education and to include them in some of the company's projects. In order to provide an explicit answer, we will first give some facts related to the curricula of bachelor programs offered to students at BMU:

- Curricula of programs in Information Technology, Software Engineering, Game Development and Information Systems are fully compliant with the recommendations of IEEE Computer Society, ACM and AIS [12- 15].
- Number of lecture hours and tutorials for most important courses are above usual values.
- BMU implements a modern education methodology where a student plays a very active role working on homework and project assignment every week during each semester.

In order to illustrate what a company can expect from its scholars during their work terms, Table IV shows a list of courses of the two most relevant bachelor programs (Software Engineering and Information Technology). They are fully compliant with IEEE and ACM recommendations [11-13].

TABLE IV
COURSES OF SOFTWARE ENGINEERING AND IT BSC PROGRAMS

S	SOFTWARE ENGINEERING	Hrs /wk	INFORMATION TECHNOLOGY	Hrs/ wk
1	CS101 Intr. to OO Programming	7	CS101 Intr. to OO Programming	7
	CS220 Computer Architecture	6	IT101 IT Fundamentals	5
	MA101 Calculus 1	5	MA103 Mathematics for IT	5
	NT111 English	4	NT111 English	4
2	CS102 Object and Data Abstraction	7	CS102 Object and Data Abstraction	7
	CS323 C/C++ Progr. Language	6	CS323 C/C++ Progr. Language	6
	CS115 Discrete Structures	5	IT210 IT Systems	5
	NT112 English 2	4	NT112 English 2	4
3	CS103 Algorithms and Data Structure	6	IT331 Computer Netw. & Comm.	5
	SE201 Introd. to Software Engineering	7	CS220 Computer Architecture	6
	IT350 Databases	6	IT350 Databases	6
	NT213 English for IT	4	NT213 English for IT	4
4	SE211 Software Construction	6	CS225 Operating Systems	5
	IT370 Human-Computer Interaction	5	IT370 Human-Computer Interaction	5
	IT255 Web Systems 1	6	IT255 Web Systems 1	6
	MA202 Calculus 2	5	CS324 Scripting Languages	6
5	SE321 SW Quality, Testing and Maiten.	6	SE201 Intr. to Software Engineering	7
	SE311 SW Design and Architecture	6	IT335 Computer Sys. & Net. Admi.	5
	SE322 Software Requirements	5	Elective Course 1	
	IT355 Web Systems 2	6	IT355 Web Systems 2	6
6	SE325 Project Mgmnt for SW Devel.	6	SE325 Project Mgmnt for SW Devel.	6
	CS225 Operating Systems	5	IT333 Wireless and Mobile Comm.	5
	Elective Course 1		IT381 Inform. Security and Safety	6
	Elective Course 2		CS330 Development of Mobile Appl.	6
7	Co-op Program (4 months,8 hrs/day)	40	Co-op program (4 months,8 hrs/day	40
	Elective Course 3 (online)	6	Elective Course 2 (online)	
	IT390 Prof. Practice & Etics (online)	5	IT390 Prof. practice & Etics (online)	5
	NT310 Prof. Communications (online)	5	NT310 Prof. Communications (onl.)	5
8	IT381 Information Security and Safety	6	Elective Course 3	
	Elective Course 4		Elective Course 4	
	SE495 Cupstone Project		IT495 Cupstone Project	
	ELECTIVE COURSES		**ELECTIVE COURSES**	
6	CS324 Scripting Languages	6	MA273 Probability and Statistics	5
6	MA273 Probability and Statistics	5	IS250 Arch of Enterprise IT Systems	6
6	CS330 Development of Mobile Appl.	6	CS322 Programming in C#	6
6	IT333 Wireless and Mobile Comm.	5	IS310 Enterprise IS	5
7	IT320 Adv. Technology Platforms	6	IT320 Adv. Technology Platforms	6
7	IS345 Management of Digital Content	6	IS345 Manag. of Digital Content	6
7	IT331 Computer Netw. & Comm.	5	OM350 Enterpreneourship	6
7	CS322 Programming in C#	6	IS330 IS Strategy and Management	6
8	SE401 SW Development Project	5		
8	OM350 Enterpreneourship	6		

After the first year, students should be able to perform simple programming tasks in Java and C++, as they had three programming courses in first two semesters:

- CS101 Introduction to OO programming (7 hrs. /wk.)
- CS102 Object and Data Abstraction (7 hrs. /wk.)
- CS323 C/C++ Programming Language (6 hrs. /wk.)

For each course, students get homework assignments each week and have to realize a project, by developing an application in Java and in C++.

After the second year, Software Engineering students should be able to perform tasks of junior Java or C++ programmers, as they have the following courses:

- CS103 Algorithms and Data Structure (6 hrs. /wk.)
- SE201 Introduction to Software Engineering (7 hrs. /wk.)
- IT350 Databases (6 hrs. /wk.)
- SE211 Software Construction (6 hrs. /wk.)
- IT370 Human-Computer Interaction (5 hrs. /wk.)
- IT255 Web Systems (6 hrs. /wk.)

After completing the Year 3, students are ready for software development projects, as they had all needed software engineering courses:

- SE321 SW Quality, Testing and Maintenance
- SE311 Software Design and Architecture
- SE322 Software Requirements
- SE325 Project Management for SW Development
- Web front-end programing (Web Systems 1) and web back-end programming (Web Systems 2). Besides CS225 Operating Systems, they also have two elective courses in Semester 6.

They have full-time (40 hrs. /wk.) working term in a company, i.e. BMU co-op partner during Semester 7. Besides studying two courses (IT381 Information Security and Safety and a elective course) the main activity in Semester 8 is the SE495 Capstone project. If a student is the scholar of a BMU co-op partner, it is expected that its future employer, BMU co-op partner, would specify its capstone project.

Having the curricula of Software Engineering, Information Technology, Game Development and Information Systems bachelor programs at BMU [11-15] in mind, we are sure that students may perform many programming tasks during their work terms in companies, BMU co-op partners.

VI. The Learning Model of BMU Co-op

The co-op education includes school-based and work-based learning. When implementing a parallel co-op model, like the BMU co-op model, it is necessary to split the students daily activities between academic courses and work in their companies. Actually, their work should be structured according to their class schedule.

When students follow a traditional, in-class academic program they have at least 20 contact (active) hours a week, or four in-class hours per working day. If the company does not operate in the same location or near the university, due to travel time of students between the university and company, the available working time, in daily basis is limited to maximum three, in average. One solution of the problem is to schedule courses is such a way that students have two days a week free for their work in companies, and three days when they have courses, with cca seven in-class hours a day, in average. This structuring model of students' activities restricts companies to use students only two days a week. This interruption of their work may disturb their work in company projects, because they normally work in teams with others fully employed team members. If they are completely out of work three days a week, these projects may be seriously affected

An alterative to traditional (in-class) mode of learning is to implement online mode of learning. In this case, co-op students would share their time between their work placement in companies and study activities at home. In this case, co-op students and companies can more easily coordinate their work and learning time. This solution is definitely better for companies, but students have to be highly motivated and well self-organized to successfully realize their on-line courses and learning at home.

BMU co-op model is offering a more appropriate mode of learning, a hybrid or blended learning. Students need to read and learn the content of online lessons, delivered by the e-learning system of BMU at home and come to the university for in-class tutorials and lab work. In this scheduling model, students spend less time at university in classes, in comparison with traditional mode of studying, but still use the benefits of direct communication with their lecturers and teaching assistants during tutorials and lab works. This is a compromise solution that combines good features of all three modes of learning:

- *On-line learning* using provided learning content gives students an opportunity to learn when they are ready for this, and they also learn how to learn alone, which they will need to do during their professional life any way.
- *In-class tutorials and lab work* provide very useful interactions of a student with other students and with lecturers and teaching assistants. This can help them to better acquire new knowledge and skills.
- *Informal learning* during their work in a company, helps a co-op student to learn something that is not normally offered in academic courses, such as technologies and working practices that are specific to the company - their future employer.

The basic features of in-class or face-to-face learning, online (e-learning) and hybrid (blended) learning are different. Fig. 6 and 7 summarize these specific features of the four learning models. We analysed the learning processes taking into account the following features:

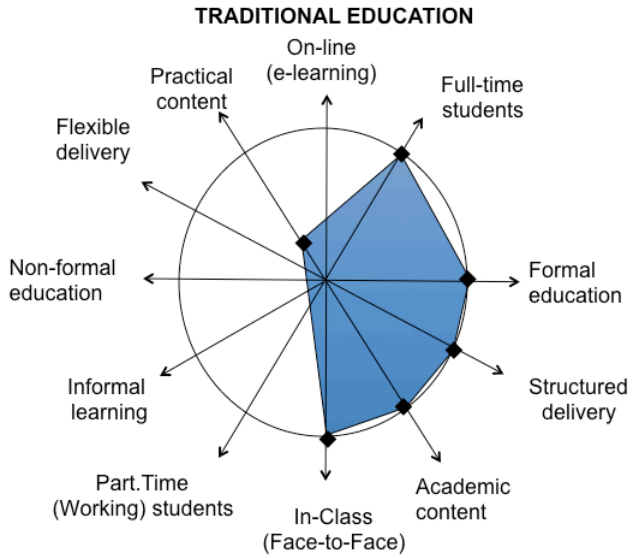
- On-line and in-class learning
- Formal, non-formal and informal education
- Full-time and part-time students
- Academic and practical learning content

- Structured and flexible delivery of learning content

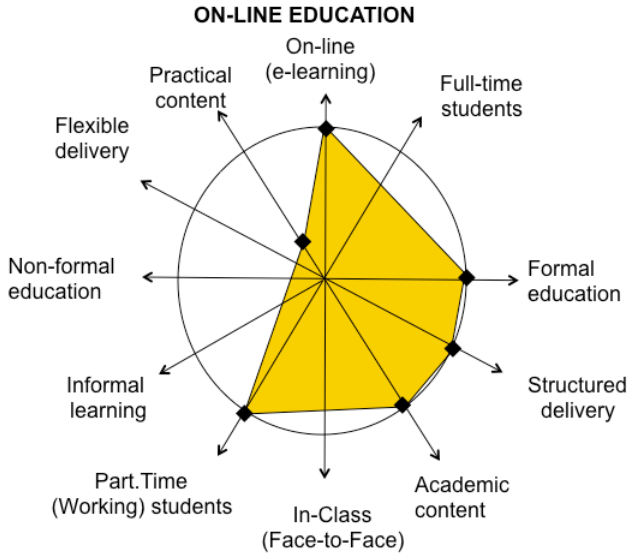
We analysed four learning models:

1. Traditional (in-class or face-to-face)
2. On-line (e-learning)
3. Hybrid 1: traditional, but student use e-learning to use learning contents.
4. Hybrid 2: Student use on-line lessons instead of traditional lectures, and have traditional, in-class tutorials and lab works.

Fig. 6 shows diagrams with typical values of these features in case of traditional (Fig. 6.a) and online education (Fig. 6.b)



a) Features of traditional education



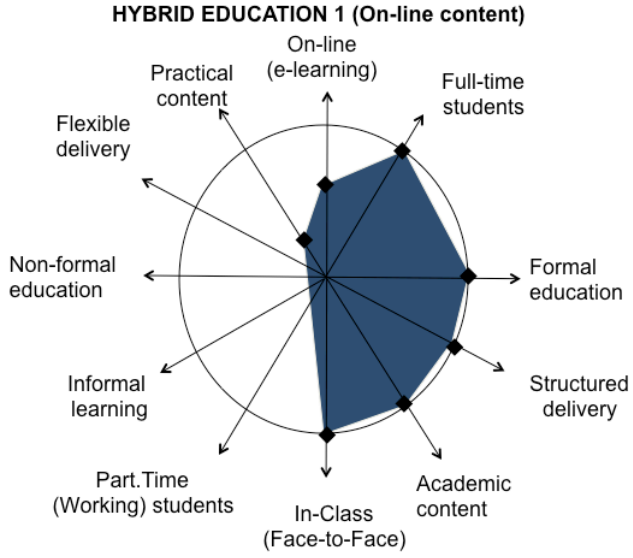
b) Features of online education

Fig. 6 Typical values of features of traditional and online education

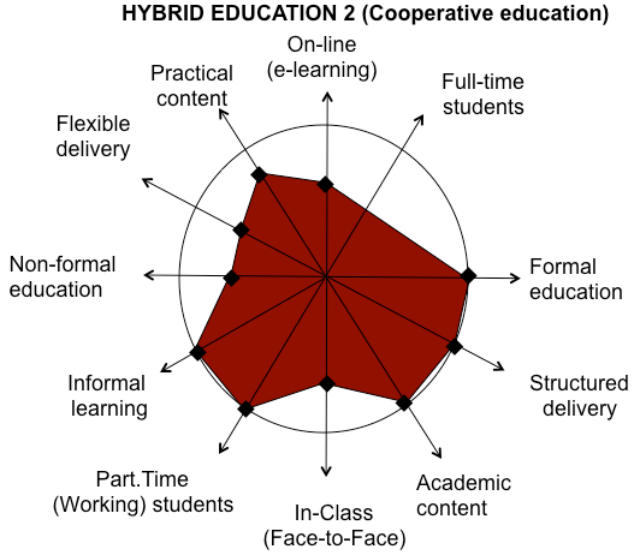
Fig. 7 shows diagrams with typical values of features in case of two hybrid models of education.

BMU is using three of these four education models:

1. **Online Education** – used for working students and students living outside Belgrade and Niš.
2. **Hybrid Education 1** – used in BMU Belgrade campus, where we offer traditional, in-class education, but students use the online content by using our e-learning system.
3. **Hybrid Education 2** – used in BMU Niš campus where we provide in-class tutorials and lab works, and students prepare themselves for tutorials by reading and analysing our online lessons and their learning contents.



c) Features of hybrid education 1



d) Features of hybrid education 2

Fig.7 Typical values of features of two hybrid educational models.

Analysing these diagrams, we can notice that the Hybrid Education Model 2 provides the richest set of features, mainly because it includes both informal and non-

formal education, and it provides a flexible delivery of learning contents. These features are missing in traditional education. The implementation of a parallel co-op model, as the BMU co-op model, requires informal and non-formal education and also allows a more flexible scheduling of education and work terms in daily basis. These are the reasons why BMU decided to adopt a parallel co-op model that implements the Hybrid Education Model 2.

VII. How does the BMU Co-op Program Work?

Companies interested in the BMU Co-op program should initiate contact with BMU to jointly analyse the specific needs of the company in order to specify the most appropriate Co-op program model.

A. Location

It is necessary to specify where co-op students should work. The best solution is to work in the same building where they are studying. BMU offers the workspace in its Business and Education Center (BEC) in Niš, and the co-op partner may rent the space for its development teams. BMU offers 2 m^2 of this space free of charge for each co-op student having financial support for its studies from the company. If located in BEC, the company should locate its experienced SW developers or IT staff which will preform its development projects, in which co-op students are also involved as team members there.

If a company prefers that co-op students work in location where the company operates, it is also acceptable by BMU. The only drawback of this solution for the co-op student is the waste of traveling time between BMU location and the company location.

B. Mentors

BMU co-op Partner Company should assign a mentor for each co-op student that will collaborate with the student's mentor from BMU. They will specify homework assignments and project topics for all BMU courses, together with lecturers of these courses. They will also select the most appropriate elective courses from company point of view.

Company mentors should also help co-op students to become familiar with the working practice of the company, and for specifying possible training for students to learn company specific technologies and know-how.

C. Selection of Students

As BMU co-op program covers all eight semesters, it is necessary to select freshmen students interested to be co-op students and scholars of a BMU co-op partner. BMU starts its marketing campaign for enrolment of new students from October till September following year, for the academic year starting 1st of October. BMU representatives visit about 200 secondary schools promoting its programs and organize many promotional events (such as workshops, free courses) and tournaments, such as "Met Mobile Challenge", "Metropolitan Talents", "It Project of the Year" etc. It is very important to start early promotion of scholarships offered by BMU co-op partner companies (from October at best), in order to attract best secondary school students for enrolment to BMU and for these scholarships. BMU and its co-op partner publish a public call for enrolment of potential students to the co-op program specified for the particular company.

BTU and its co-op partner specify selection criteria for enrolment and scholarships (including paid tuition fees) and a selection procedure. Usually candidates are asked to be tested and to solve some logical problems and programming tasks (based on a given online short training course). The company and BMU representatives then interview successful candidates. The final decision regarding accepting a candidate is on the company.

BMU and its co-op partner company make a contract with each student enrolled in the co-op program specified for the company. The contract specifies all requirements and obligations of all three parties.

- A *student* is obliged to work for the company for at least four years upon graduation, if a job is offered to them. They must acquire 60 ECTS each year and get the average mark 8,00 (of 10.00) or higher. If a student shows poor performance, the company may cease the contract and stop paying the tuition fee and scholarship.
- *The company* normally pays tuition fees for each academic year for the student and specified scholarships. The company should also provide working conditions and project for students during its working time in the company.
- *BMU* takes the responsibility to provide academic courses and to coordinate work assignments of the co-op students with its co-op partner company.

D. Contract Between BMU and its Co-op Partner

BMU prepares and signs a contract with each of its co-op partners, specifying all details regarding their role and obligations in the co-op program specified for each co-op partner. As companies may have different needs and requirements, a specific co-op program is specified for each of them, but based on the general BMU co-op framework program. The contract should specify the amount of scholarships, the number of enrolled scholars for each academic year, terms and conditions for rental of working space (if it is rented) etc.

VIII. Benefits to Program Partners

Our co-op programs provide the following benefits to

program partners:

IT Company-BMU Co-op Partner:

- Annually employs new graduated IT or software engineers, its scholars, educated according to their needs (in numbers and with appropriate qualifications).
- Return of investment (ROI) in education of its future employees – its scholars - is shorter then their studies. It means that the revenue of the company based on the work of its scholars is higher then the cost of their education (paid tuition fees and scholarships).

Co-op Student – Scholar of the Company gets:

- Free education, as the company pays its tuition fees.
- A scholarship.
- A good job upon graduation
- The best from both formal education (BMU courses) and informal leaning (working in a company in parallel with its formal education).

BMU:

- Enrols better students, as it can offer them a good package (free education, scholarship and job upon graduation).

Fig. 8 shows some of these benefits:

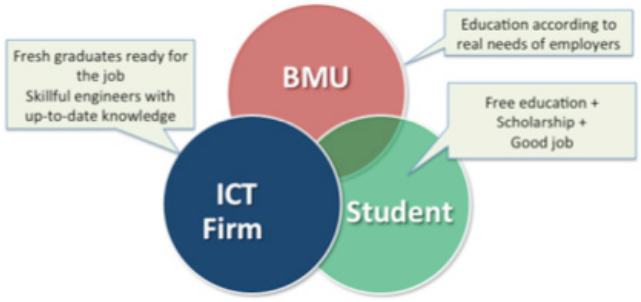


Fig. 8 Some of benefits to partners of the co-op program

VIII. Conclusion

The co-operative education program of BMU is based on some specific features (such as simultaneous education and work placement of co-op students) and provides obvious benefits to all three partners (win-win-win):

- *A IT company* - BMU co-op partner, have a stable annual employment of new graduate IT and software engineers, educated according to its needs by investing in their education according to a cost-effective co-op model.
- *A co-op student* gets free education (paid tuition fee), a scholarship and a good job upon graduation.
- *BMU* enrols better students and can implement its mission more easily– to provide a quality education that satisfies the needs of employers.

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On the Implementations of Circuit Models of Arcs

Simon Le Blond, Brian Ross, and Vančo Litovski

Abstract - Fault arc models are increasingly important for design of modern power system protection algorithms. Several solutions were reported in the literature but no comparisons of the behaviour were given. Furthermore, in fact, while all models are based on solving a differential equation where the conductance of the arc is unknown, not much of the conductance was reported the main concerns being oriented towards the voltage, current and power of the arc. This paper thus initially presents electrical circuits that implement existing arc model equations. Namely, a circuit in which one node voltage equals the arc conductance is developed for every model. These then were simulated and the resulting arc conductances are reported and compared here.

Keywords - arcing, arc modelling, arc simulation, circuit model

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1. INTRODUCTION

Arcing faults in power systems can cause considerable damage, even explosions, despite the installed protection system [1] [2]. In fact numerous failures occurring in these systems may be attributed to arcing which in its initial stage leads to fault currents between two conductors. Depending on the parameters of the electrical network, such as power source and equivalent impedance, these failures may lead to stable arcs provided both the protection system fails to activate and no self-extinguishing process is started. After arc extinction and reenergizing the system, the phenomenon can reappear, depending on the level of the driving voltage and the load current, and also depending on the performance of the partly damaged insulation, characterized by its thickness and chemical composition.

Thus the diagnosis and location of such a fault when it occurs or, even better, correct prediction before it fully develops, is of prime importance for proper maintenance and protection of the power distribution system. Crucial to the development of any diagnostic and fault prediction system is a simulator that supplements difficult, disruptive, and expensive experiments on real LV power systems. Vital to the simulator, in turn, are models that capture the properties of the specific components of the system and when instantiated behave as faithfully as the real components as possible. Such models must be accurate, so one may depend on the simulation results; must be robust, putting no limits to realistic signal's amplitudes and waveforms; must be simple, enabling fast simulation of complex systems to which the modelled device belongs; and be easy to represent in software in a form convenient for frequent instantiation.

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One may now categorize the existing models, already mentioned in the Introduction, into the following groups:

1. The high impedance model (HI), described by an equation of the form

(1) $G(t)=f(G_0,\tau,t)$;

2. The models describing electro-thermal dynamics of the arc described by an equation of the form

(2) $$\frac{1}{G(t)}\cdot\frac{dG(t)}{\mathrm{d}t}=f(G_0,\tau,\mathbf{c},i(t),v(t),P(t))\,,$$

c being a set of constants;

3. The non-equilibrium models described by an equation of the form

(3) $$\frac{1}{G(t)}\cdot\frac{dG(t)}{\mathrm{d}t}=f\left(G_0,\tau,\mathbf{c},i(t),v(t),P(t),\frac{dv(t)}{dt}\right),$$

and

4. The model involving ablation described by an equation of the form

(4) $$\frac{1}{G(t)}\cdot\frac{dG(t)}{\mathrm{d}t}=f\left(G_0,\tau,\mathbf{c},i(t),v(t),P(t),L(t),S(t)\right).$$

The following notation was used: t for the time variable, G for the arc conductance, G_0 for its initial value, $i(t)$ for the arc current, $v(t)$ for the arc voltage, $P(t)$ for the arc power, $L(t)$ for the arc length, and S(t) for the arc area.

From electrical modelling and simulation point of view there is a fundamental difference between the first one and the last three. Namely, if the HI model is to be implemented the arc conductance will start with zero (open circuit) and will rise to a prescribed value (G_0) no matter what happens with the currents and voltages. In the rest of the cases the conductance stars with some initial value (which may be high) and, depending on the model and the model parameters, rises or decreases in time.

The existing models as given in the literature [3] [4] [5] [6] were first studied from the applicability in a circuit form. Having in mind that (3) in fact represents one differential equation containing time derivatives of two different variables we first excluded (3) as candidate for circuit modelling. Then, we supposed that the arc length and the arc area are constant reducing (4) into (2). Therefore, (1) and (2) were left and used for further study.

Electrical circuits convenient for implementation in circuit simulators recognizing behavioural descriptions were developed for every single arc model found in the literature. These were then simulated while excited by a sinusoidal voltage source of amplitude of 380 V and of power frequency of 50 Hz having internal resistance of 1 mΩ. As a simulation results the solutions of (1) or (2) were taken and demonstrated here. To make the comparison adequate equal or similar parameter values were used for different model in the largest possible extent.

Since, to our best knowledge, no reports of this kind were published we consider the results depicted below as an asset to build on, so no special comments on the appropriateness of any of them were given.

The analysis will follow the order already established in the literature such as [4] [5]. To get feeling as to what are the differences between the models and to save space simulation results will be given on one figure only.

It is important to note that these models were developed with an intention to simulate arcs in the open (including air, vacuum, and oil as an environment). That means they are supposed to be fed by a source of very low resistance. To allow for that, in the simulations reported here, internal resistance of the proper voltage source of 1 mΩ was used.

The paper is structured so that the models are visited in succession and circuits are proposed for each one of them. Then simulation results are given collectively.

2. Creation of the Arc Model and Simulation Results

In this section a review of the existing models will be given. For every one of them a circuit will be proposed that enables implementation of the model within a circuit simulator.

2.1 The high impedance model (HI)

A time varying conductance reported in [6] and implemented also in [7] [8] [9] may be used to model the arc occurring between two power lines or between a line and ground. Namely, it is proposed that the arc conductance is obeying the following differential equation

$$\frac{\mathrm{d}G(t)}{\mathrm{d}t} = \frac{1}{\tau}(G_0 - G(t)) \tag{1}$$

where G_0 and τ are model parameters.

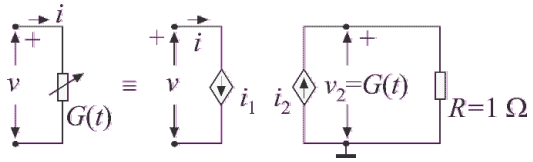

Figure 1. Resistive circuit modelling the nonlinear conductance given by (2)

The solution of this equation is

$$G(t) = G_0(1 - \mathrm{e}^{-t/\tau}). \tag{2}$$

As can be seen, in this case, the value of the arc conductance at the beginning of arcing is zero, meaning infinite resistance, and ends up at the end of the arcing process with the value G_0 which is a model parameter usually obtained by measurement. τ is the other parameter which may here be interpreted as the time constant of the arcing and, again, obtained by measurement.

This conductance may be modelled by the circuit of Fig. 2 where

$$i_1 = v \cdot v_2 \tag{3}$$

$$i_2 = G_0(1 - \mathrm{e}^{-t/\tau}). \tag{4}$$

We assume that the arcing starts not at the very beginning of the simulation which means that the time variable in (1) is not the real time but a new variable shifted to the arcing instant. To create a time variable that starts with zero at t_0 and ends with $\Delta t = t_1 - t_0$ at t_1 the circuit of Fig. 2 may be used.

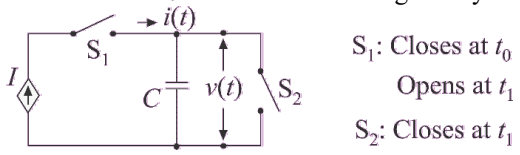

Figure 2. A circuit generating a voltage proportional to time. $t_1 > t_0$.

For this circuit one may state that

$$v(t) = \begin{cases} 0 & \text{for } t < t_0 \\ \dfrac{I}{C}(t - t_0) & \text{for } t_0 < t < t_1 \\ 0 & \text{for } t > t_1 \end{cases}. \tag{5}$$

Here t_0 is the time instant when the fault occurs while $\Delta t = t_1 - t_0$ is the duration of the fault. One may say that a protective device was activated (or some other remedial action was undertaken) at t_1. In that way, if we substitute t by $v(t)$ in (4), we will have a time dependent conductance that starts changing at t_0 and falls back to zero at t_1.

In the subsequent simulation experiments t_0=50 ms, t_1=150 ms and C=1 F were used.

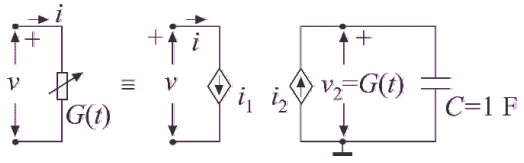

Figure 3. Electrical circuit generating the solution of the differential equation governing the arcing process

In order to unify the simulation, however, instead of using

the closed form expression for the conductance given by (2) we will use a circuit that solves the differential equation (1) during the simulation. To that end the circuit of Fig. 3 was used. In this case we have

(6a) $$i_1 = v \cdot v_2$$

(6b) $$i_2 = \frac{1}{\tau}(G_0 - G(t)) \cdot$$

To implement the model for verification and testing purposes we used the circuit depicted in Fig. 4. It consists of a sinusoidal source with internal resistance R_0, and a switch that activates the arc at $t=t_0$ and deactivates it at $t=t_1$.

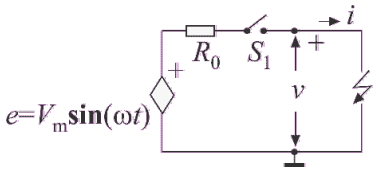

Figure 4. The simple circuit used for verification and characterization of the model

The simulation results for this type of arc model are depicted in Fig. 5 (denoted by 1). G_0=100 S and τ=0.04 s were used.

2.2 The Cassie model

This model was first published in [10]. It is expressed in the following form:

(7) $$\frac{1}{G(t)} \cdot \frac{dG(t)}{dt} = \frac{1}{\tau}\left(\frac{v^2}{V_c^2} - 1\right).$$

Note that since, at $v(0)=0$,

(8) $$\frac{1}{G(0)} \cdot \frac{dG(t)}{dt}\Big|_{t=0} = -\frac{1}{\tau},$$

$G(0)$ determines the initial value of the conductance (which is not specified by the model as such), while $-G(0)/\tau$ represents its slope at the origin. Accordingly, the model is defined by three parameters: τ, V_c, and $G(0)$.

With reference to Fig. 3, in this case we have

(9a) $$i_1 = v \cdot v_2$$

(9b) $$i_2 = -\frac{1}{\tau} \cdot v_2 + \frac{1}{\tau \cdot V_c^2} \cdot v_2 \cdot v^2 .$$

The value of $G(t)$ corresponding to the one expressed by (7), obtained by running the circuit of Fig. 4 by SPICE, is depicted in Fig. 5 denoted by 2. The following parameters were used for this simulation: R_0=1 mΩ, G_0=100 S, τ=10 ms, and $V_C^2 = 1000$ V.

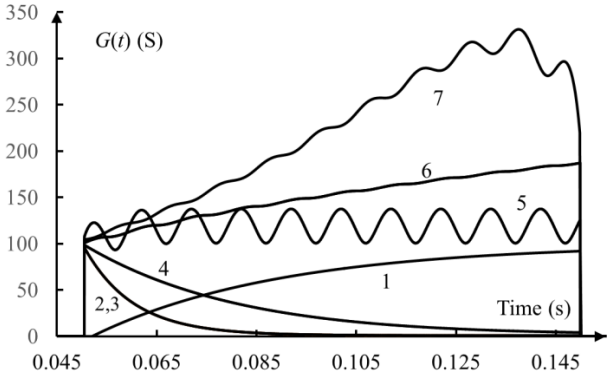

Figure 5. Conductance $G(t)$ for various models
1. High impedance model
2. Cassie model
3. Schewemacher model
4. Schwarz model
5. Mayr model
6. Modified Mayr model
7. Habedank model

It is important to note that Equ. (9) has a solution

(10) $$G(t)=G(0)\cdot e^{-t/\tau}$$

even in the absence of any voltage at the arc terminals. That means that exponential decay of the arc conductance is expected since, after breakdown, one may expect $v(t)<V_c$ or even $v(t)<<V_c$ and (10) is practically governing the process.

It also means that, in the case of a short duration of the arc, the time of activation of the arc should be set to zero at the activation moment and, after the arc is extinguished, the capacitor (In Fig. 3) should be short-circuited to discharge.

2.3 The Schwarz arc model

The Schwarz arc model [11] may be expressed as:

(11) $$\frac{1}{G(t)} \cdot \frac{dG(t)}{dt} = \frac{1}{\tau \cdot G^a(t)}\left(\frac{v \cdot i}{P \cdot G^b(t)} - 1\right).$$

where P is the cooling constant, while a and b are constants. It is a four parameter model which may be stated as a black-box since the parameters a and b have no physical interpretation. a and b are in fact fitting parameters.

For circuit simulation it will be expressed schematically on the same way as the Cassie circuit i.e. by Fig. 3, while the corresponding current sources will be expressed in the following way

(12a) $$i_1 = v \cdot v_2$$

(12b) $$i_2 = -\frac{1}{\tau} \cdot v_2^{1-a} + \frac{1}{\tau \cdot P} \cdot v_2^{1-a-b} \cdot v \cdot i$$

The value of $G(t)$ corresponding to the one expressed by (11), obtained by running the circuit of Fig. 4 by SPICE, is

depicted in Fig. 5 denoted by 4. The following parameters were used for this simulation: R_0=1 mΩ, G_0=100 S, τ=100 ms, and P=1 W, a=0.1 and b=0.15.

2.4 Model Mayr model and modified Mayr

This model was frequently implemented [11] [12] [13] [4].

The original Mayr equation is as follows:

$$\frac{1}{G(t)}\cdot\frac{dG(t)}{\mathrm{d}t}=\frac{1}{\tau}\left(\frac{v^2(t)G(t)}{P_0}-1\right). \tag{13}$$

Using the circuit of Fig. 3 one may express the model as

$$i_1=v\cdot v_2 \tag{14a}$$

$$i_2=-\frac{1}{\tau}\cdot v_2+\frac{1}{\tau\cdot P_0}\cdot v_2^2\cdot v^2. \tag{14b}$$

The value of $G(t)$ corresponding to the one expressed by (13), obtained by running the circuit of Fig. 4 by SPICE, is depicted in Fig. 5 denoted by 4. The following parameters were used for this simulation: R_0=1 mΩ, G_0=100 S, τ=10 ms, and P=100 W.

The modified Mayr model [14] is described by the following equation

$$\frac{1}{G(t)}\cdot\frac{dG(t)}{\mathrm{d}t}=\frac{1}{\tau}\left(\frac{v(t)\cdot i(t)}{P_0+C\cdot|i|}-1\right). \tag{15}$$

The corresponding controlled sources of Fig. 3, now are

$$i_1=v\cdot v_2 \tag{16a}$$

$$i_2=-\frac{1}{\tau}\cdot v_2+\frac{1}{\tau}\cdot v\cdot i\cdot\frac{v_2}{P_0+C\cdot\sqrt{i^2}} \tag{16b}$$

The value of $G(t)$ corresponding to the one expressed by (15), obtained by running the circuit of Fig. 4 by SPICE, is depicted in Fig. 5 denoted by 6. The following parameters were used for this simulation: R_0=1 mΩ, G_0=100 S, τ=10 ms, C=50 V, and P=1000 W.

2.5 The Habedank Model

The model equations proposed by Habedank [15] are

$$\frac{1}{G_\mathrm{c}(t)}\cdot\frac{dG_\mathrm{c}(t)}{\mathrm{d}t}=\frac{1}{\tau_\mathrm{c}}\left(\frac{v^2(t)G^2(t)}{V_\mathrm{c}^2G_\mathrm{c}^2(t)}-1\right) \tag{17a}$$

$$\frac{1}{G_\mathrm{m}(t)}\cdot\frac{dG_\mathrm{m}(t)}{\mathrm{d}t}=\frac{1}{\tau_\mathrm{m}}\left(\frac{v^2(t)G^2(t)}{P_0G_\mathrm{m}(t)}-1\right) \tag{17b}$$

$$\frac{1}{G(t)}=\frac{1}{G_\mathrm{c}(t)}+\frac{1}{G_\mathrm{m}(t)} \tag{17c}$$

where $G_\mathrm{c}(t)$ is the arc conductance in the Cassie equation, τ_c is the Cassie time constant, $G_\mathrm{m}(t)$ is the arc conductance in the Mayr equation, τ_m is the Mayr time constant and P_0 is a constant. In fact here one has *two nonlinear time dependent mutually coupled conductances in a system with six free parameters*: τ_c, V_c, $G_\mathrm{c}(0)$ and τ_m, V_m, $G_\mathrm{m}(0)$. That is a serious challenge from the parameter extraction and implementation point of view since positive feedback may be set for some combination of the parameters.

To get the circuit representation of this series connection we will first substitute resistances in place of the conductances. In that way the Habedank model will be expressed as

$$-\frac{1}{R_\mathrm{c}(t)}\cdot\frac{dR_\mathrm{c}(t)}{\mathrm{d}t}=\frac{1}{\tau_\mathrm{c}}\left(\frac{v^2(t)\cdot[R_\mathrm{c}(t)+R_\mathrm{m}(t)]^2}{V_\mathrm{c}^2\cdot R_\mathrm{m}^2(t)}-1\right) \tag{18a}$$

$$-\frac{1}{R_\mathrm{m}(t)}\cdot\frac{dR_\mathrm{m}(t)}{\mathrm{d}t}=\frac{1}{\tau_\mathrm{m}}\left(\frac{v^2(t)\cdot[R_\mathrm{c}(t)+R_\mathrm{m}(t)]^2}{P_0\cdot R_\mathrm{m}(t)\cdot R_\mathrm{c}^2(t)}-1\right) \tag{18b}$$

$$R(t)=R_\mathrm{c}(t)+R_\mathrm{m}(t). \tag{18c}$$

For a given port voltage (v) the solution of this pair of equations is obtained as the port current (i) of the circuit depicted in Fig. 6.

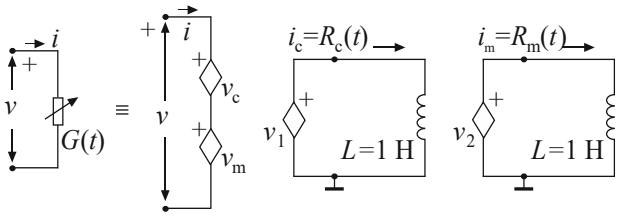

Figure 6. Circuit implementing the Habedank arc model

Here we have

$$v_\mathrm{c}=i\cdot R_\mathrm{c}(t) \tag{19a}$$

$$v_\mathrm{m}=i\cdot R_\mathrm{m}(t) \tag{19b}$$

$$v_1=\frac{dR_\mathrm{c}(t)}{\mathrm{d}t}=\frac{R_\mathrm{c}(t)}{\tau_\mathrm{c}}\left(1-\frac{v^2(t)}{V_\mathrm{c}^2}\frac{[R_\mathrm{c}(t)+R_\mathrm{m}(t)]^2}{R_\mathrm{m}^2(t)}\right) \tag{19c}$$

$$v_2=\frac{dR_\mathrm{m}(t)}{\mathrm{d}t}=\frac{R_\mathrm{m}(t)}{\tau_\mathrm{m}}\left(1-\frac{v^2(t)}{P_0}\frac{[R_\mathrm{c}(t)+R_\mathrm{m}(t)]^2}{R_\mathrm{m}(t)\cdot R_\mathrm{c}^2(t)}\right) \tag{19d}$$

The value of $G(t)$ corresponding to the reciprocal of the one expressed by (18), obtained by running the circuit of Fig. 4 by SPICE, is depicted in Fig. 5 denoted by 7. The following parameters were used for this simulation: G_0=100 S, $\tau_\mathrm{c}=\tau_\mathrm{m}$=100 ms, and P_0=1000 W, $V_\mathrm{c}^2=1000$ V², $R_\mathrm{c}(0)=R_\mathrm{m}(0)=10$ mΩ.

2.6 The Schavemaker model

The Schavemaker model [14] is described by the following equation

$$(20)\quad \frac{1}{G(t)}\cdot\frac{dG(t)}{dt}=\frac{1}{\tau}\cdot\left(\frac{v(t)\cdot i(t)}{\max\left(V_{\text{arc}}\cdot|i|,P_0+C\cdot v(t)\cdot i(t)\right)}-1\right).$$

This model is specific since it uses an approximating function with discontinuous derivative. From that point of view it is interesting and challenging for circuit implementation.

For implementation of this model one may use the circuit of Fig. 3 again with the following:

(21a) $i_1=v\cdot v_2$

$$(21c)\quad i_2=-\frac{1}{\tau}\cdot v_2+\frac{1}{\tau}\cdot v\cdot i\cdot\frac{1}{\max\left(V_{\text{arc}}\cdot\sqrt{i^2},P_0+C\cdot v\cdot i\right)}.$$

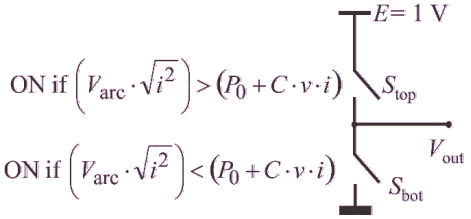

Figure 7. The comparator

To complete the circuit a comparator is needed producing an output voltage V_{out} such that

$$(22a)\quad V_{\text{out}}=1 \text{ if } \left(V_{\text{arc}}\cdot\sqrt{i^2}\right)>\left(P_0+C\cdot v\cdot i\right),$$

(22b) $V_{\text{out}}=0$, otherwise.

Based to that the current i_3 was calculated as

$$(23)\quad i_3=\frac{1}{V_{\text{out}}\cdot\left(V_{\text{arc}}\cdot\sqrt{i^2}\right)+\left(1-V_{\text{out}}\right)\cdot\left(P_0+C\cdot v\cdot i\right)}.$$

The comparator circuit used to create V_{out} of (22) is depicted in Fig. 7.

The value of $G(t)$ corresponding to the reciprocal of the one expressed by (18), obtained by running the circuit of Fig. 4 by SPICE, is depicted in Fig. 5 denoted by 3. The following parameters were used for this simulation: τ=10 ms, P_0=100 W; C_{int}=50 V_{arc}=1000 V G_0=100 S.

4. Conclusion

Implementation of the arc model equation in a form of electrical circuit is of crucial importance from the simulation point of view. Namely, when such circuit models are available, fault simulation is enabled for complex power systems including bus-bars, switchgears, power lines, cables, transformers etc. That in turn allows for successful design and maintenance of the grid.

Various models proposed in the literature were implemented here and simulated by the SPICE simulator. It is important, however, to have in mind here that the models described may be used in any circuit simulator allowing for behavioural controlled sources to be used.

The simulation results show that by using different models different real-life situations may be captured and proper simulation to be performed. Having that in mind one is not in situation to give any recommendations or comparison of the model described as far.

5. Acknowledgements

This work is part of the Innovate UK Energy Catalyst project, SYNAPS (Synchoronous Analysis and Protection System). The authors gratefully acknowledge the joint financial support of EPSRC and Innovate_UK and use of facilities and services at the University of Bath, UK.

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Self-Heating Assessment for Interconnects During ESD Event

Vazgen Melikyan, Ararat Khachatryan and Davit Mirzoyan

Abstract –During ESD event the metal interconnects can be impacted due to Joule heating. A self-heating model for metal interconnects has been proposed for providing a realistic assessment of current and interconnect performance during ESD event. This model is matching with experimental results, and it can be used to forecast TLP I(V) characteristics of isolated metal wires.

Keywords – Interconnects, self-heating, ESD event, Joule heating.

I. Introduction

During ESD event a high Joule heating is a major cause of failure in metal interconnects and this could be enhanced by using of low-k material as interlayer dielectric, since such materials exhibit poor thermal properties. In fact, the increase in current densities in metallic interconnections, and the subsequent self-heating are particularly destructive [1,4]. ESD discharges can cause both latent and permanent damages in interconnections. In metal based interconnect the self heating effect leads to permanent resistance change and reduces the electromigration lifetime significantly [5,6]. Moreover, as the temperature variation increases the metal lines resistance [8,9], the voltage drop across the ESD protection path is strongly impacted. Thus, it is crucial for supporting ESD designers to develop a scalable compact model able to take self-heating effect into account and included a failure criterion in order to predict the transient and quasi-static behavior of an interconnection as well as its failure [1,6]. In order to provide a realistic assessment of current and future interconnect performance, a self heating model for isolated metal lines, valid in the ESD time range, is developed. This model will be compared experimental results in 45nm and 130nm technology, and it will be used to forecast TLP I(V) characteristics of isolated metal wires

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II. Interconnect Model

A. Model Equations

Since the increase in temperature of a metal line seems to be the main parameter accountable of the failure, in many works authors have sought to simulate the temperature rise due to Joule self-heating in the metal line. In the HBM to CDM time domain the adiabatic assumption cannot be applied and the heat diffusion in the dielectric has to be taken into account. Contrary to [1, 9] which use a thermal RC network with a constant thermal capacitance, [2] assumes that there is a volume of dielectric within a thermal diffusion length (not constant during the transient event) which is at the same temperature as the metal. By solving the heat equation (1), which links the temperature T and the current density j of the considered material, [2] establishes the expression of the total thermal capacitance of an interconnection (2).

$$\rho * c\left(\frac{\partial T}{\partial t}\right) = \nabla(k * \nabla T) + \rho_e(T) * j^2 \qquad (1)$$

Where ρ is material density, ρ_e electrical resistivity, c specific heat and k thermal conductivity.
The total thermal capacitance is the sum of the thermal capacitance of the metal, C_{THM}, and the thermal capacitance of the dielectrics enclosing it, C_{THD}:

$$C_{TH}=C_{THM}+C_{THD} \qquad (2)$$

Where

$$C_{THM}=c_M*V_{METAL} \qquad (3)$$

$$C_{THD}=c_{IMD}*V_{IMD}+ c_{ILD}*V_{ILD} \qquad (4)$$

c_M, c_{IMD} and c_{ILD} are respectively the specific heat coefficients of the metal interconnect, the inter-metal dielectric (IMD) and the inter-layer dielectric (ILD) as illustrated in the figure 1.

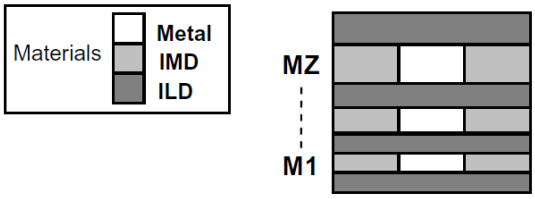

Fig. 1. Cross section of metal layers stacked

The heat conduction volumes of each material, V_{METAL}, V_{IMD} and V_{ILD}, depend on the interconnect geometrical specifications, L, H and W, as shown in figure. As the dielectrics heat conduction volumes are calculated from the interconnects dimensions in order to have a scalable model, two shape factors s_L for the IMD and s_v for the ILD, are introduced.

$$V_{METAL}=L*H*W \quad (5)$$
$$V_{IMD}=2s_L*L*H*W_{DIFF} \quad (6)$$
$$V_{ILD}=2s_VL*W*H_{DIFF} \quad (7)$$

W_{DIFF} and H_{DIFF} are respectively the thermal diffusion lengths of the IMD and the ILD as illustrated in the figure 2.

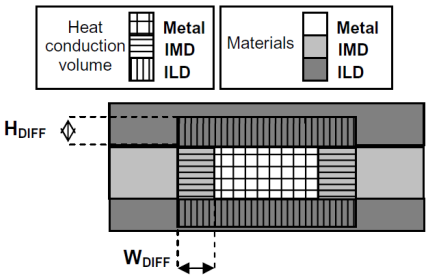

Fig. 2. Cross section of a metal layer during the heat dissipation

Those dimensions are directly linked to the time and the thermal diffusion coefficients of the inter-metal dielectric, α_{IMD}, and the inter-layer dielectric, α_{ILD}, following those equations:

$$W_{DIFF} = \sqrt{\alpha_{IMD} t} \quad (8)$$
$$H_{DIFF} = \sqrt{\alpha_{ILD} t} \quad (9)$$

The temperature variation is directly linked to the electrical energy dissipation, E, and thermal capacitance of the interconnection, C_{TH}:

$$E(t) = C_{TH} * \Delta T(t) \quad (10)$$

The energy needed to increase the system temperature is provided by Joule heating (11).

$$E(t) = \int_0^{\Delta t} R(t) i^2(t) dt \quad (11)$$

Then, the metal resistivity dependence with temperature has been assumed to be linear. Thus, a temperature variation, _T, leads to a variation of the interconnect resistance, R, according to the following equation:

$$R = R_0(1 + TCR \times \Delta T) \quad (12)$$

R_0 is the resistance value at the reference temperature and TCR is the temperature coefficient resistance. [3] asserts that resistance increases linearly with the energy, even through the metal phase change from solid to a liquid, whereas, [1] uses two different TCR values, one corresponding to the solid phase of the metal line and the second to its liquid phase. In this paper there is chosen one TCR coefficient which is sufficient to model accurately the linear resistor variation during the transient event (figure 8). The resistance R0 is defined by the metal resistivity, ρ, and the geometrical specifications of the interconnection: the length, L, the height, H and the width, W, as depicted in the figure 1:

$$R_0 = \rho \frac{L}{H*W} \quad (13)$$

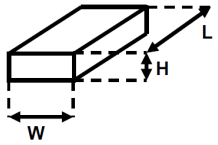

Fig. 3. Geometrical specifications of an interconnection

In order to have a scalable model of self heating the equivalent thermal capacitance is defined by the interconnect dimensions as:

$$C_{TH}(t) = \left(c_M + c_D\delta(t)\right) * L * H * W \quad (14)$$

Where

$$C_D = c_{ILD} + c_{IMD}$$
$$\delta(t) = \sqrt{\alpha_D t} \quad (15)$$

The α_D parameter integrates the thermal diffusion coefficients and the shape factors of heat conduction volumes of the dielectrics.

B. Metal failures under high current short pulses

Metal wires exposed to ESD stresses, and more generally to short-time high current pulses, show thermally accelerated open circuit failures [2]. The temperature rise in interconnect appears to be the main parameter which controls the metal failure. In [3] there is shown that the failure temperature of a passivated metal line should be included between its melting temperature (660 °C) and its evaporation temperature (2467 °C). Experimentally, [2] uses the DC resistance thermometry to assess the temperature rise in passivated metal wire. Based on element simulations and measurements, there is shown that the metal open always occurs at the same temperature rise, which is over 1000 °C. As the copper melting temperature is 1084 °C [1] and according to [6], it is supposed that the critical temperature leading to an open failure is above this value. All these considerations have lead to introduce the metal melting temperature, T_{MAX}, in the model as a failure criterion. If the metal line temperature exceeds this limit the interconnection resistance takes an infinite value. The impact of multiple stresses on the resistance is not taken into account in the model. Nevertheless, a second temperature threshold can be

introduced in order to take into account the reliability reduction by sending a warning message to caution designers that latent damages can appear in interconnections. This temperature threshold can be linked to the current level that causes an electromigation lifetime reduction [5] (around 50% of the failure current). After having defined the failure criterion, the scalability of the αD parameter should be examined.

III. Parameter Extraction

The specific heat coefficients, the resistivity and the height of the interconnection is technological data. The 45nm and 130nm technology nodes information were used as an experimental results. In order to extract the parameter αD, a methodology based on the following steps must be used on transient characterizations as illustrated in figure 4.

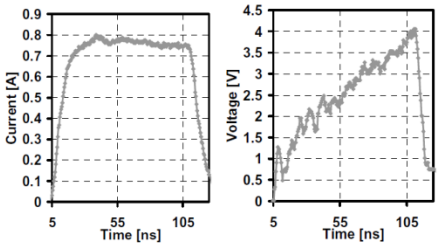

Fig. 4. Voltage and current chronograms of an interconnection for a TLP voltage pulse with a 100ns duration.

First, it's necessary to calculate the energy and the temperature during the transient event as (figure 5):

$$E(t) = \int V(t)I(t)dt \tag{16}$$

$$\Delta T(t) = \frac{1}{TCR}\left(\frac{\frac{V(t)}{I(t)} - R_0}{R_0}\right) \tag{17}$$

Knowing, the specific heat coefficient and the interconnects dimensions, the function δ(t),depicted in figure 6, can be calculated as :

$$\delta(t) = \frac{1}{c_D}\left(\frac{1}{L*H*W}\frac{E(t)}{\Delta T(t)} - C_M\right) \tag{18}$$

Finally, αD can be extracted easily from the δ(t) curve.

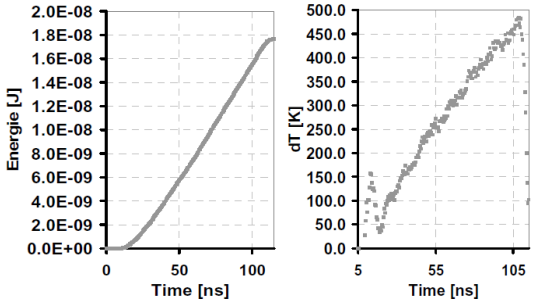

Fig. 5. Energy and temperature chronograms of an Interconnection (TLP voltage pulse, 100ns duration)

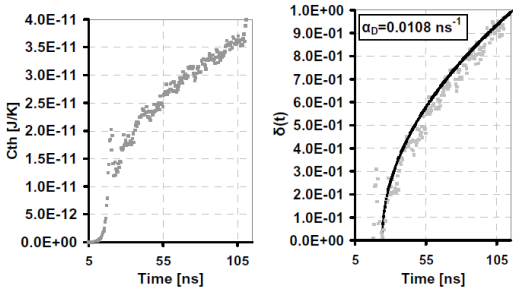

Fig. 6. Equivalent thermal capacitance and function δ(t) of an interconnection (TLP voltage pulse, 100ns duration)

The extraction results presented in figure 7 show that αD only depends of the metal layer and also of the interconnect height. The value of αD is sensibly equal for M1 and MX metal layer. This is due to the metal thickness which is the approximately the same for those metal layers as the dielectrics around the interconnections. As the thickness of the metal layer MZ is higher than the M1 layer thickness the dielectrics volume used for the heat dissipation is smaller than the metal volume which is bigger due to its thickness. As the dielectrics contribution concerning the heat dissipation is smaller the αD value of the MZ layer is clearly lower. The width seems to have few impacts on the αD parameter.

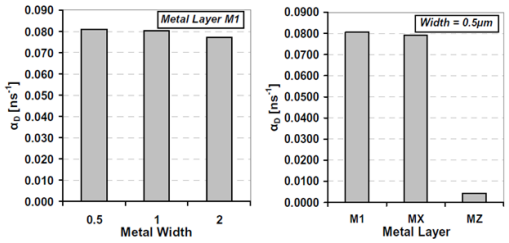

Fig. 7. α_D coefficient value for different widths of metal layers

IV. Validation

As depicted in figure 8, the simulated voltage of an interconnection fits perfectly the measurement data for a TLP voltage pulse with 100ns duration. It can be concluded that the self-heating effect is correctly reproduced during the transient event.

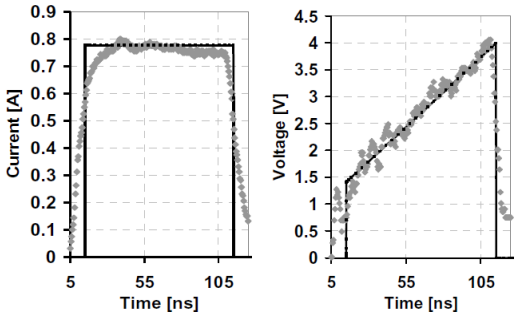

Fig. 8. Voltage and current chronograms of an Interconnections (TLP voltage pulse, 100ns duration) Measurement – Gray, simulation – Black

Then, simulations corresponding to TLP and VF-TLP characterizations using a 50_ impedance were performed for different pulse duration (100ns, 30ns, 10ns) as illustrated in the figures 9, 10 and 11. The averaging window applied on simulated chronograms and measurements for each TLP pulse is defined between 60% and 80% of the pulse duration. By applying this averaging of each simulated pulse we have built the TLP IV curves. The simulated results provided by the compact model are well correlated with measurements.

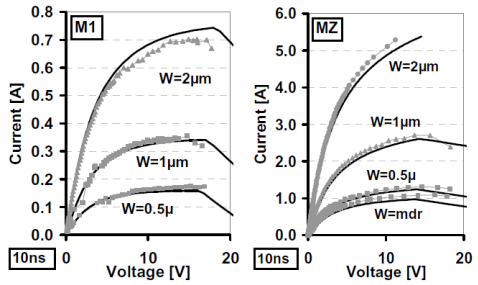

Fig. 9. VF-TLP IV curves of interconnections, 45nmtechnology: two metal layers M1 and MZ, measurements Gray and simulations Black for 10ns square pulses

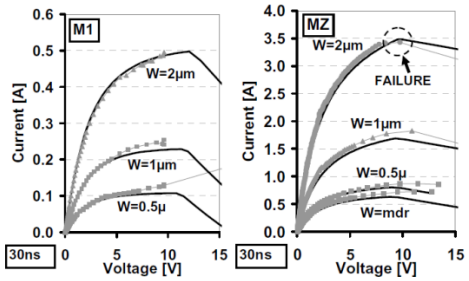

Fig. 10. VF-TLP IV curves of interconnections, 45nm technology: two metal layers M1 and MZ, measurements-Gray and simulations Black for 30 ns square pulses

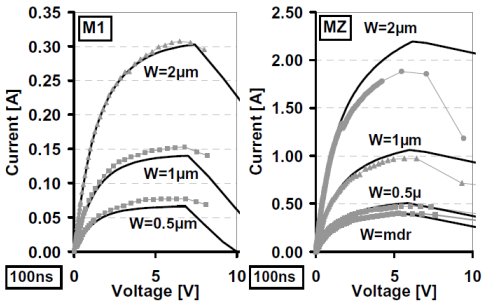

Fig. 11. VF-TLP IV curves of interconnections, 45nm technology: two metal layers M1 and MZ, measurements - Gray and simulations - Black for 100 ns square pulses.

Then, when the interconnection reaches the metal melting temperature the model resistor has a high value in order to reproduce an open circuit failure as explained in II.B. Thus, it is observed a kink in simulated curves. As the metal melting temperature provides a good estimation of the interconnects failure, it can be considered as a valuable failure criterion.

VI. Conclusion

High Joule heating during ESD event is a major cause of failure in metal interconnects. To provide a realistic assessment of current and future interconnect performance, a compact model of self heating in isolated metal lines, valid in the ESD time range (time <100ns), has been proposed. The results with this model matching with experimental results performed in 45nm and 130nm technology, and it can be used to forecast TLP I(V) characteristics of isolated metal wires.
Moreover this model only required the extraction of a single model parameter for each metal layer. Without a complete thermal RC network on contrary with [1, 9], but using only a thermal capacitance the model provides a matching with measurements maximum by 9% tolerance and a prediction concerning the failure by 5% tolerance.

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3D Modeling and Simulation of the Tesla's Polyphase Generators and Motors

Vladan Vučković

Abstract - This paper presents the 3-D modeling and simulation of the Tesla's poly-phase generators and machine using original real-time simulator. Models and simulations of Tesla's alternating current generators and induction motors based on his rotating magnetic field are presented. Power transformers and rotating magnetic field that is invented by Tesla is the basic concept of his poly-phase system for producing, transferring and utilization of the alternating electric energy.

Keywords - 3d modeling and simulation, rotating magnetic field, Tesla's induction motor.

I. INTRODUCTION

Project *Computer Simulation and 3-D Modeling of the Original Patents of Nikola Tesla* started in April 2009 in cooperation with the Faculty of Electronics in Niš and a Nikola Tesla Museum form Belgrade. The aim of the project realized by the Faculty of Electronic Engineering in Niš is multiple. Basically, it deals with detailed 3-D modeling [1],[2] of the original patents of Nikola Tesla, which are the part of the Museum's archives. Using 3-D models, further objectives are rendering, animation, simulation and visualization of the different machines in real time. One of the basic intentions is to simulate some of the fundamental Tesla's invention in the field of power generating and utilization using alternating currents. The main invention in Tesla's poly-phase system is his invention of the *rotating magnetic field*. This invention enables the realization of the induction motors without commutators - feature that is very useful for industry. Nikola Tesla invented this in 1882, in a moment of inspiration. A few years later, he patented basic concepts of his new poly-phase system in US.

This paper presents basic details about the 3d modeling, simulation and realization of the models of Tesla's generators and motors using the concept of the rotating magnetic field in improved version of author's original particle simulator. The user is able to monitor these machines in real time and tune some parameters of the alternating currents in stators. Also, we simulate the complete work of the tree-phase generators and induction motors with the original 3D engine. Simulator could visualize the movements of the rotor in induction motor as well as magnetic field itself near the engine model.

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II. THE IDEA OF ROTATING MAGNETIC FIELD

The invention of the rotating magnetic field in terms of practical and industrial use is the work of Nikola Tesla [3],[4]. The Italian electrical engineer Galileo Ferraris accidentally stumbled on the effect of rotation in the field with two spools and current difference of 90 degrees, but not found the right value effect. Tesla is exhibited in his autobiography that he found a rotating field in early 1882. In 1888, Tesla was awarded US patent (US Patent 381.968) for his invention. From the first concept of rotating fields there was a series of practical inventions of the early types of motors and generators, which were later found their application in industry [4]. The Tesla fundamental patents are presented in following diagrams (Fig.1).

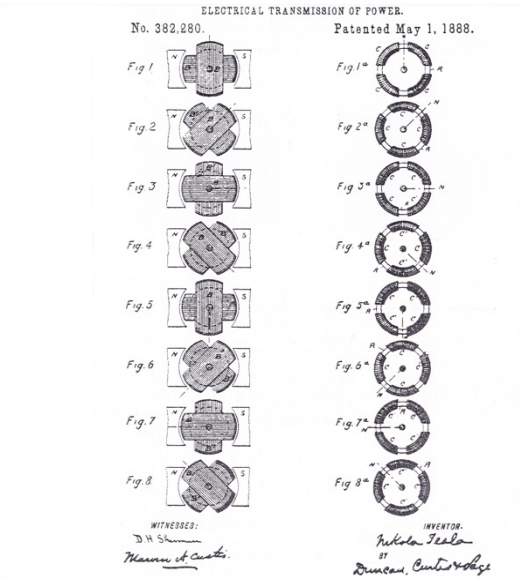

Fig.1. Fundamental concept of rotating magnetic field (US patent 382.280).

In Fig.1. Tesla described all key positions of rotor into the rotating magnetic field motor. To achieve rotating

someone does not need to use commutators or other switch devices. Through this patent Tesla postulated a basic principle for transmission of the electrical energy using the alternating poly-phase currents. The first poly-phase engine and the concept of the first motor that Tesla has built as the practical demonstration of his invention is based on this patent. The generator uses the rotating permanent electro magnet producing alternating currents with different phases. The presented motor uses alternating current with phase difference of 90 degrees, energizing two different poles of it. The stator has common iron core and four electro-magnets. The rotor is simple and is made of iron or some other ferromagnetic material. *There is no commutator*. These phase-differenced currents generate rotating magnetic field in stator that moves the rotor. This is also asynchronous machine; the speed of rotation is similar but under the virtual speed of the rotating field.

Studying these engines, we can observe that the magnetic flux is placed around the stator in near proximity of the machine. The inner space (rotor) is also under magnetic influence of the stator, so rotating magnetic field is driving (hanging) the rotor in fact.

The next scheme (Fig.2.) presents the poly-phase alternator (generator). This machine is able to generate two phase currents in two separate circuits. The stator is constructed with eight groups of inductors and the rotor has two electro or permanent magnets. In Tesla system, inductors are connected in stator part of machine. The rotation of the magnets generates two phase alternating current.

The other conception of this generator is also presented. In this case, the rotor is in the constant magnetic field generated by the permanent magnet in stator. The rotation of the inductions in the center of the machine generates two alternating currents with the phase difference of 90 degrees.

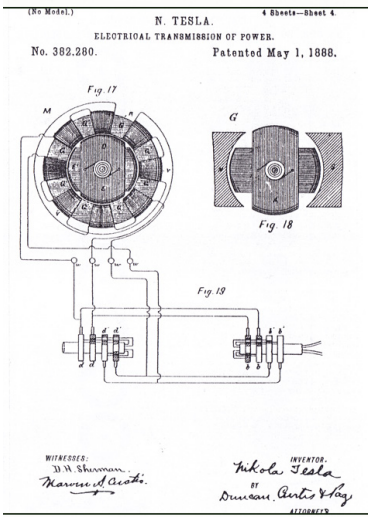
(No Model.) 4 Sheets—Sheet 4.
N. TESLA.
ELECTRICAL TRANSMISSION OF POWER.
No. 382,280. Patented May 1, 1888.
Fig. 17
Fig. 18
Fig. 19
WITNESSES:
INVENTOR.
Nikola Tesla
BY
ATTORNEYS.

Fig.2. Original Tesla's U.S. patent 382.280; alternator for two-phase currents.

Now, these currents could drive the two phase rotating magnetic field engine that is earlier presented. We could notice here Tesla's conception is general. He invented not only the principle of the rotating magnetic field but also the generators (alternators), the principle of using poly-phase transformers and different kinds of the motors based on same principle. The simplest variation oh Tesla's system is two-phase system, but the same idea could be realized with three or more phases. Nowadays, the modern Tesla system is commonly three-phase, including alternators, transformers and induction motors. This variant of the Tesla's system is proved as optimal and it is widely used for more of 100 years.

III. MODELING THE MOTORS AND GENERATORS

On the basis of Tesla's patents, we have developed a 3D model first, and then the simulation of engine [5]. We use standard tools like Autodesk 3dsMax and Maya, with the programmed action of the 3D force field vector.

In the first phase, we constructed wire models [6]. We developed some complex models of different Tesla machines: generators, motors and transormers (Fig 3a-c).

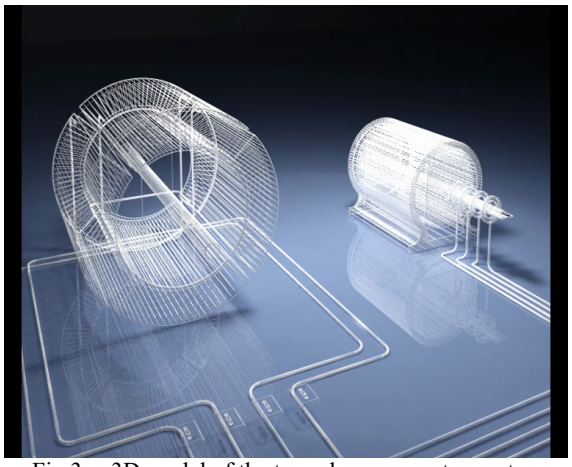

Fig.3a. 3D model of the two-phase generator-motor.

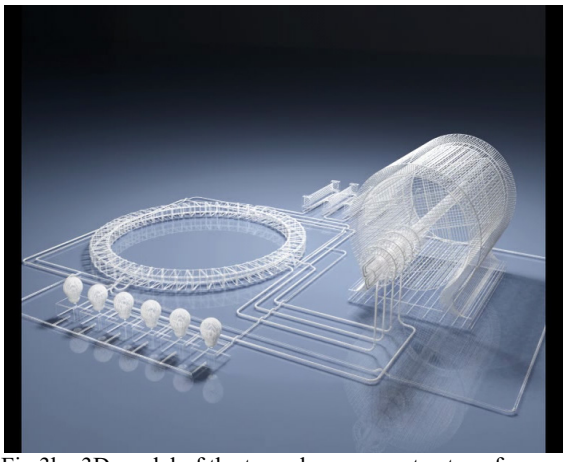

Fig.3b 3D model of the two-phase generator-transformer.

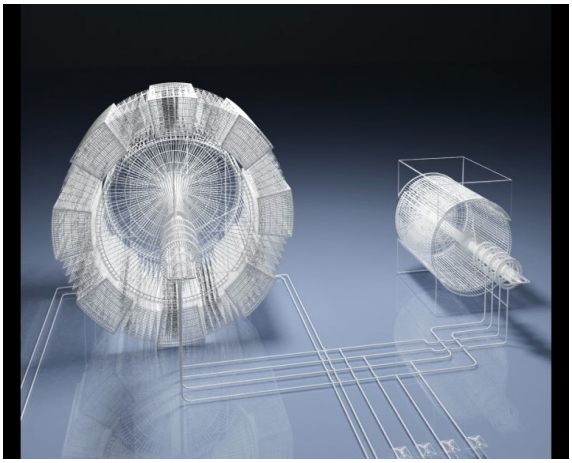

Fig.3c. 3D model of the three-phase generator-motor.

The stators and the rotors are clearly separated in all motors. Rotors are provided for rotation around the central axis. In transformer models, the lights are connected to motors. In the next phase the materialization taking into account the metal magnetic pieces and copper conductors. In the end, we merged the generator and motor conductors in the model, following the patent applications (Fig.4.).

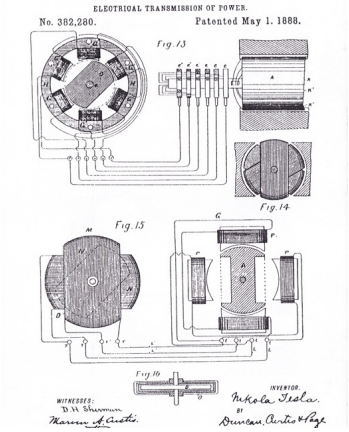

Fig.4. Tesla patent of induction generator-motor system with wiring.

The correspondent 3D model is presented in Fig.5a.b.

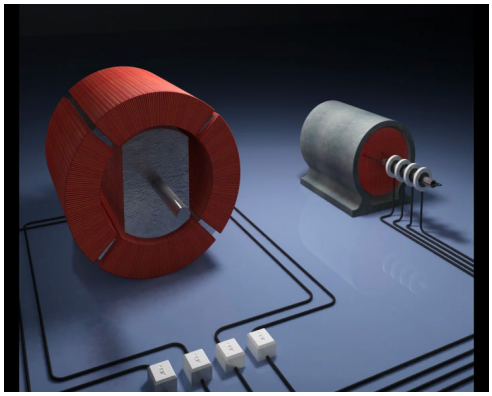

Fig.5a. Two-phase induction motor-generator 3D model.

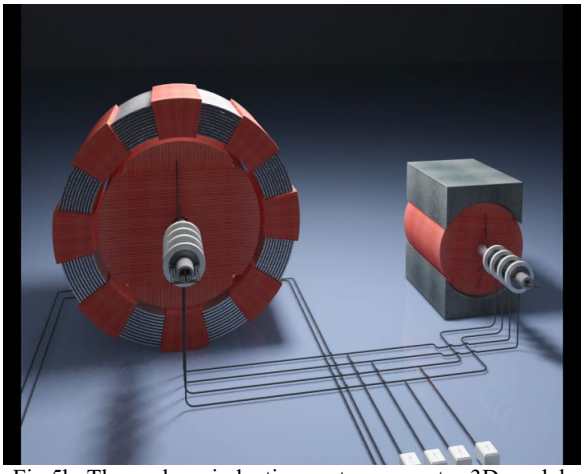

Fig.5b. Three-phase induction motor-generator 3D model.

An important model to simulate was Tesla symetric motor-generator. There are two identical machines symetricly connected. One machine could act like generator and the other like motor and vice-versa (Fig. 6.a.b.).

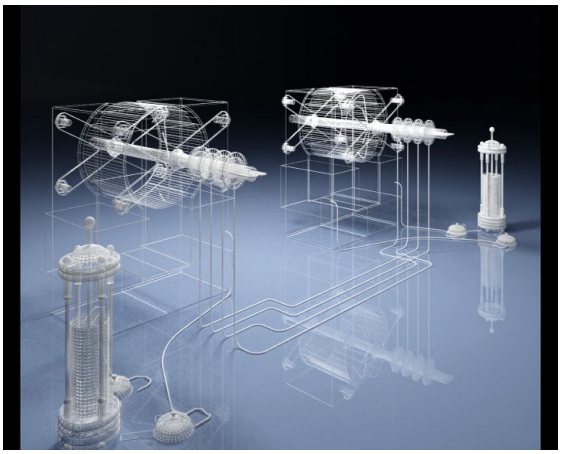

Fig.6a. Two phase symmetric induction motor-generator 3D wire model.

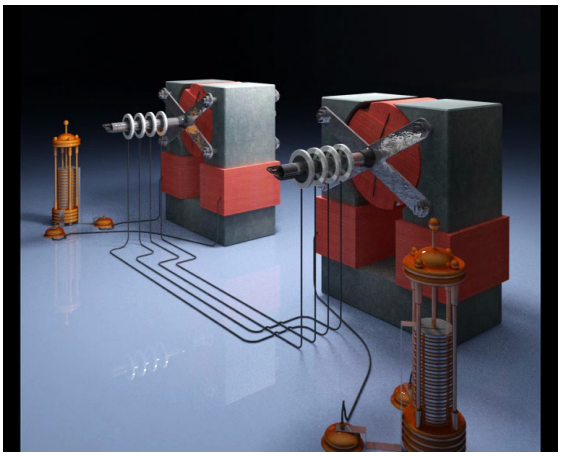

Fig.6b. Two phase symmetric induction motor-generator 3D model.

There is no limitation to implement this procedure. We realized and presented tens of Tesla's models.

IV. SIMULATION

After the preliminary phases we have complete generator-motor model. Model must follow the basic functionality of the Tesla's patent, so we must define the rotation of the alternating generator, the transmission and rotation of the induction generators and motors. In the next figure (Fig.7.) we presented simulation of 2-phase alternator-motor.

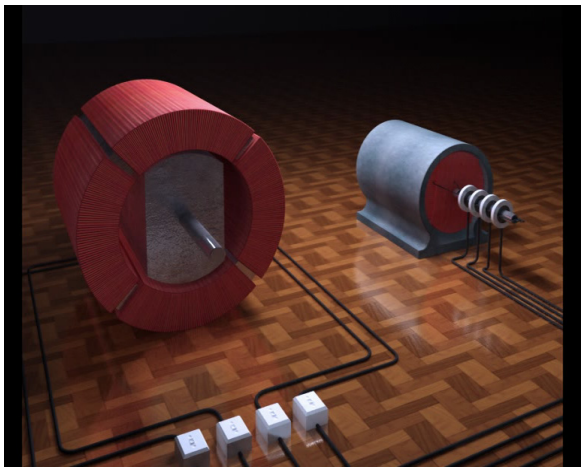

Fig.7. Simulation of two-phase alternator-motor system.

This model is actually correspondent with the schematic version in Tesla's patent, consisting of permanent magnetic rotor, iron stator and eight copper inductions. The materials are also carefully chosen having in mind the functionality of this device [7]. Rotation speed is also controlled in simulation. Alternator produces alternating currents developing the rotating magnetic field in motor (Fig. 8).

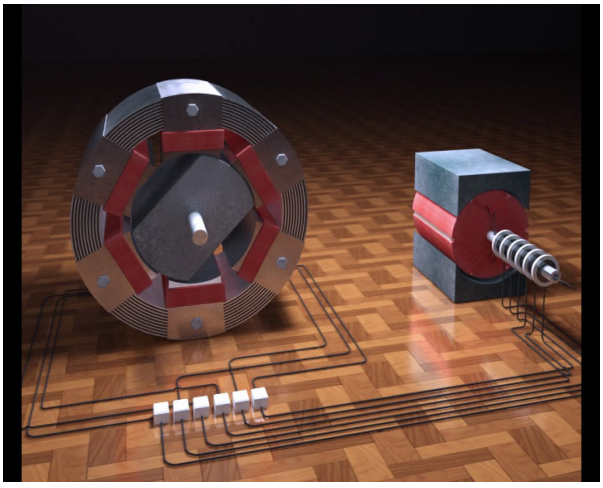

Fig.8. Simulation of three-phase alternator-motor system.

We also use proper wiring to support the total functionality of the model. Of course, the modeling of the current flow in conductors is very complex and it is not needed in this work, but on higher level we also use the current modeling, separately in all wires. The virtual currents are in function of phase of alternator.

In the next figure (Fig.9) the wiring in model is presented. All of these wires are under different virtual voltage, so system performs the simulation on this level. When start to rotate the generator, the model follows the currents and then it generates the virtual rotating magnetic field that is presented visually in model.

The change of the rotation direction in alternator generates the different virtual currents in opposite rotation of the rotor in motor, with time delay.

In alternator-transformer-lights simulation, alternator generates two-phase currents through transformer and then fires the lights (Fig. 9).

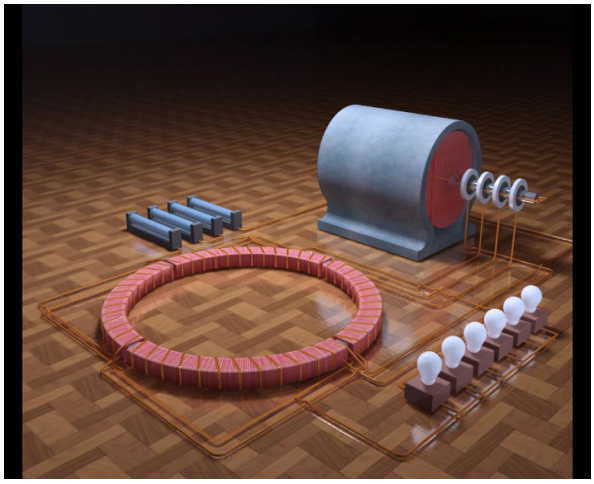

Fig.9. Alternator-transformer simulation.

V. REALIZATION

Generally, simulation of the processes is realized through the standard 3D environment.

In the special cases, like quantum or field effect Delphi 7 programming environment could be used for manual programming.

We use classical approach and first define data record as the array of quantum information:

```
...
type_elec = record
            x,y:real;     {x and y coordinates}
            vx,vy:real;   {Real velocity}
            q,m:real;     {Mass and electric charge}
            {.}
            newx,newy:integer;   {New video coordinates}
            oldx,oldy:integer;   {Old video coordinates}
```

```
        {.}
        mass:integer;
        {.}
       end;

var T: array [1..num] of type_elec;  {main array}
...
```

For instance, the main simulator line used in our system could be defined in this procedure:

```
procedure SIMULATOR_LINE(Sender: TObject);
begin

 stoping:=false;

 REPEAT
   {.}
   GENERATOR;
   {.}
   ELECTROt;   {Electrostatic field influence}
   MAGNETt;  {Magnetic field influence}
   {.}
   LIMITt;  {Space limits}
   {.}
   MOVEt;   {Move particles}
   TRANSt;  {Change physical coordinates}
   VIEWt;   {View}
   {.}
   application.ProcessMessages;
   {.}
 UNTIL stoping;

end;
```

The next listings define 3 main procedures in our simulator:

```
{-----------------------------------------------------}
{Electrostatic field influence}
{-----------------------------------------------------}

procedure ELECTROt;
var deltavx,deltavy:real;
begin
  for i:=1 to num do
  begin
    {deltavx:=t[i].q*EX*deltat/t[i].m;}
    deltavy:=t[i].q*(EY+ESTAT)*deltat/t[i].m;
    {.}
    {t[i].vx:=t[i].vx+deltavx;}
    t[i].vy:=t[i].vy+deltavy;
  end;

end;

{-----------------------------------------------------}
{Magnetic field influence}
{-----------------------------------------------------}

procedure MAGNETt;
var deltavx,deltavy:real;
begin
  for i:=1 to num do
  begin
    deltavx:=t[i].q*BB*t[i].vy/t[i].m;
    {deltavy:=t[i].q*BB*t[i].vx/t[i].m;}
    {.}
    t[i].vx:=t[i].vx+deltavx;
    {t[i].vy:=t[i].vy+deltavy;}
  end;
end;

{-----------------------------------------------------}
{Moving the particles}
{-----------------------------------------------------}

procedure MOVEt;
var realx,realy,dsr:real;
begin
  for i:=1 to num do
  begin
    realx:=t[i].vx*deltat;
    realy:=t[i].vy*deltat;
    {.}
    t[i].x:=t[i].x + realx;          {move x}
    t[i].y:=t[i].y + realy;          {move y}
    {.}
    {.}
{x levo}  if (t[i].x<1) then begin t[i].x:=maxx-1; end;
{x desno} if (t[i].x>maxx) then begin t[i].x:=1; end;
      {.}
{y levo}  {if (t[i].y<1) then begin t[i].y:=maxy-1; end;
{y desno} {if (t[i].y>maxy) then begin t[i].y:=1; end;}
      {.}
{y}     if (t[i].y<=1) then begin t[i].vy:=-(t[i].vy/3);
t[i].y:=t[i].y - realy; end;
{y}     if (t[i].y>=maxy-1) then
                begin
                  t[i].vy:=-(t[i].vy/3);
                  t[i].y:=t[i].y - realy;
                  {.}
                  dsr:=random(down_speed_reductionn);
                  {.}
                  dsr:=dsr+1;
```

```
            {.}
            t[i].vx:=t[i].vx/dsr;
          end;
      {.}
  end;
end;
```

The basic idea is to use a step-by-step simulator. All particles in a field are subject to the effects of electrostatic and magnetic forces and their speed depending of these forces. In each cycle simulator done to change the position by the action of a force that can be controlled by special controls.
In this way the simulator works in real-time.

V. CONCLUSION

This paper presents the complete procedure of generating 3D models and simulations of different types of Tesla's generators and engines.

The first phase is the study of the basic patents of Nikola Tesla in connection with generators and motor based on the principle of rotating magnetic field [7],[8]. In the next phase, we started the materialization of a model adding the basic functionality of generator and engine. The models of generator-motor system are running in accordance with Tesla's patent application. The next phase is materialization of the 3d models of machines using appropriate software and information about the materials.

In this way we were able to simulate the work of the generator-motor systems as well other Tesla's machines. Over 30 models has been already realized according the project.

ACKNOWLEDGEMENT

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Pspice Model for Three Phase Induction motor

Nebojša Mitrović, Vojkan Kostić, Milutin Petronijević, Bojan Banković

Abstract - PSPICE program packages are widely used in the area of electronics, but these programs can be used to simulate electrical machines and electromechanical systems. In this paper a systematic procedure is proposed for simulation of a three phase induction motor using a circuit analysis package called PSPICE. The modelling technique can be used to represent other DC and AC electric machines.

Keywords - Induction motor, electromechanical system, PSPICE.

I. INTRODUCTION

Transient analysis of electrical machines is traditionally performed by solving a system of differential equations. These equations are usually based on two-axes model of the machine. The solution lead to the required performance for various operating conditions. This process is very hard and user is ocupated by mathematics rather than getting a feel for the transient behaviour of the machine. Transient analysis of electrical machines supplied from variable frequency voltage source and current source inverters is more complicated because of the complexity of power electronic circuit. An alternative method in dealing with transient cases is the use of available CAD (Computer Aided Design) software package, for example, PSPICE.

Possibility of the PSPICE software package application on simulation of induction motor is presented in this paper. This paper introduce no new equations or new theory about induction machine modelling. Instead it illustrates a systematic procedure in order to study the behaviour of the motor using PSPICE. Investigation is also extended to determine this behaviour for different operating conditions.

II. INDUCTION MOTOR MODEL

Considerable research over the years has been devoted to the mathematical modelling of induction motors, using both frequency-domain and time-domain representations. The Frequency-domain motor representations are limited to steady-state motor performance studies. Time-domain representation can be used for both steady-state and transient performace studies. Whilst it is possible to develop a motor model in the physically existing 3-phase (or 3 axis) reference frame the presence of the mutual inductance terms, which are nonlinear functions of rotor positions, make model extremely and computationally inefficient. Since it is generally recognised [1, 2] that the two axis motor model can be used in the vast majority of operational circumstances, and is considerably less complex compared to the 3-phase model.

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The 2-axis machine equations [1, 2, 3] can be formulated in various reference frames including: stator-fixed axis, rotor fixed axis, synchronously-rotating axis and variable-speed axis, each of which has advantages depending upon the machine geometry, excitation, and operational modes under study. It is of course theoretically possible to produce a equivalent circuit for the motor based on any of these reference frames.

The three-phase induction motor terminals are connected to the electric distribution network or to the power electronic converter. Terminal instantaneous phase voltages are v_a, v_b and v_c. By choosing a stationary reference frame we have the simplest equations. We can derive the *d*-axis time varying stator side voltage v_{ds} and *q*-axis stator side voltage v_{qs} by using the following axis transformation:

$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ v_{s0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} \quad (1)$$

where v_{s0} is the possible zero sequence voltage component. The zero-sequence component does not exist in balanced three phase cases.

Axis transformation for rotor circuit is:

$$\begin{bmatrix} v_{qr} \\ v_{dr} \\ v_{r0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\beta & \cos(\beta - \frac{2\pi}{3}) & \cos(\beta + \frac{2\pi}{3}) \\ \sin\beta & \sin(\beta - \frac{2\pi}{3}) & \sin(\beta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{ar} \\ v_{br} \\ v_{cr} \end{bmatrix} \quad (2)$$

where $\beta = \theta - \theta_r$. For stationary reference frame θ=0 and

$$\theta_r = \int_0^t \omega_r dt + \theta_r(0). \quad (3)$$

After axis transformation we have the following stator voltage equations for both axis:

$$v_{qs} = \frac{2}{3}\left(v_{as} - \frac{1}{2} v_{bs} - \frac{1}{2} v_{cs} \right) \quad (4)$$

$$v_{ds} = \frac{1}{\sqrt{3}}\left(v_{bs} - v_{cs}\right) \tag{5}$$

$$v_{0s} = \frac{1}{3}\left(v_{as} + v_{bs} + v_{cs}\right) \tag{6}$$

Voltage equations for the *qd*0 axis are:

$$v_{qs} = r_s i_{qs} + \frac{d\Psi_{qs}}{dt} \tag{7}$$

$$v_{ds} = r_s i_{ds} + \frac{d\Psi_{ds}}{dt} \tag{8}$$

$$v_{0s} = r_s i_{0s} + \frac{d\Psi_{0s}}{dt} \tag{9}$$

$$v_{qr} = r_r i_{qr} + \frac{d\Psi_{qr}}{dt} - \omega_r \Psi_{dr} \tag{10}$$

$$v_{dr} = r_r i_{dr} + \frac{d\Psi_{dr}}{dt} + \omega_r \Psi_{qr} \tag{11}$$

$$v_{0r} = r_r i_{0r} + \frac{d\Psi_{0r}}{dt} \tag{12}$$

where r_r is rotor resistance, r_s is stator resistance and ω_r electrical angular speed of the rotor. Rotor voltage exist only for double fed induction motor. For singly fed machines the rotor voltage iz zero. Latest terms in the rotor side voltage equations $\omega_r \psi_{qr}$ and $-\omega_r \psi_{qr}$ are so-called rotation voltages. They are due to the rotation with respect to the stationary reference frame fixed to the stator.
Flux linkages component are:

$$\Psi_{qs} = L_{ls} i_{qs} + L_m i_{qm} \tag{13}$$

$$\Psi_{ds} = L_{ls} i_{ds} + L_m i_{dm} \tag{14}$$

$$\Psi_{0s} = L_{ls} i_{0s} \tag{15}$$

$$\Psi_{qr} = L_{lr} i_{qr} + L_m i_{qm} \tag{16}$$

$$\Psi_{dr} = L_{lr} i_{dr} + L_m i_{dm} \tag{17}$$

$$\Psi_{0r} = L_{lr} i_{0r} . \tag{18}$$

The voltage and flux linkage equations suggest the equivalent circuit shown in Fig.1.

The angular speed of the rotor ω_r is not constant in transient situations. It can be related to torque balance as:

$$T_e - T_m = J\frac{d\omega_m}{dt} \tag{19}$$

where T_e is the momentary electrical torque and T_m is the load mechanical torque.

The electric torque can be written by using the components of the stationary reference frame:

$$T_e = \frac{3}{2} pL_m\left(i_{qs} i_{dr} - i_{ds} i_{dr}\right) \tag{20}$$

The stationary frame model is very suitable to be used in circuit simulator. The synchronous angular velocity is not needed to be given for the simulator model since the equations used do not contain this variable. This is useful when we simulate a variable stator frequency motor drive.

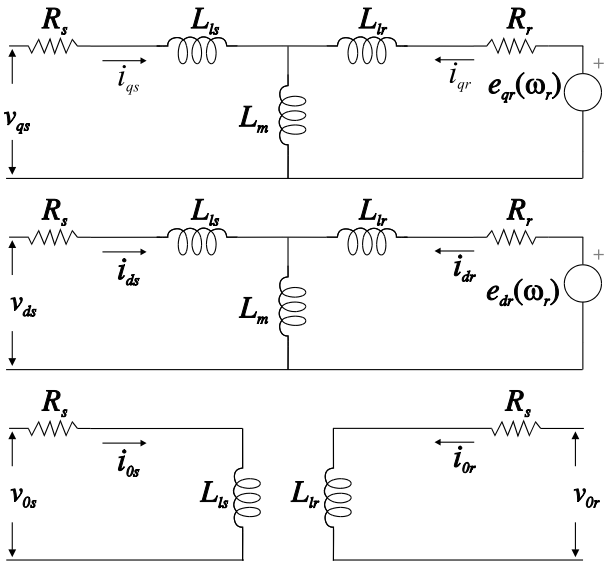

Fig.1. Induction motor equivalent circuit

III. PSPICE INDUCTION MOTOR MODEL

The developed induction motor model which is adjusted to the specific requirements of the PSPICE program package is shown in Fig. 2. Motor terminals A, B and C are conected to nodes *ua*, *ub* and *uc*.

The *qd0*-axis stator voltages are ABM blocks (Analog Bihavioural Modeling) [4] whose output voltage expression are given by Eqs. (2), (3) and (4):

2/3*(*V*(*ua*)-0.5*V*(*ub*)-0.5*V*(*uc*)),

(-*V*(*ub*)+*V*(*uc*))/*sqrt*(3),

1/3*(*V*(*ua*)+*V*(*ub*)+*V*(*uc*)).

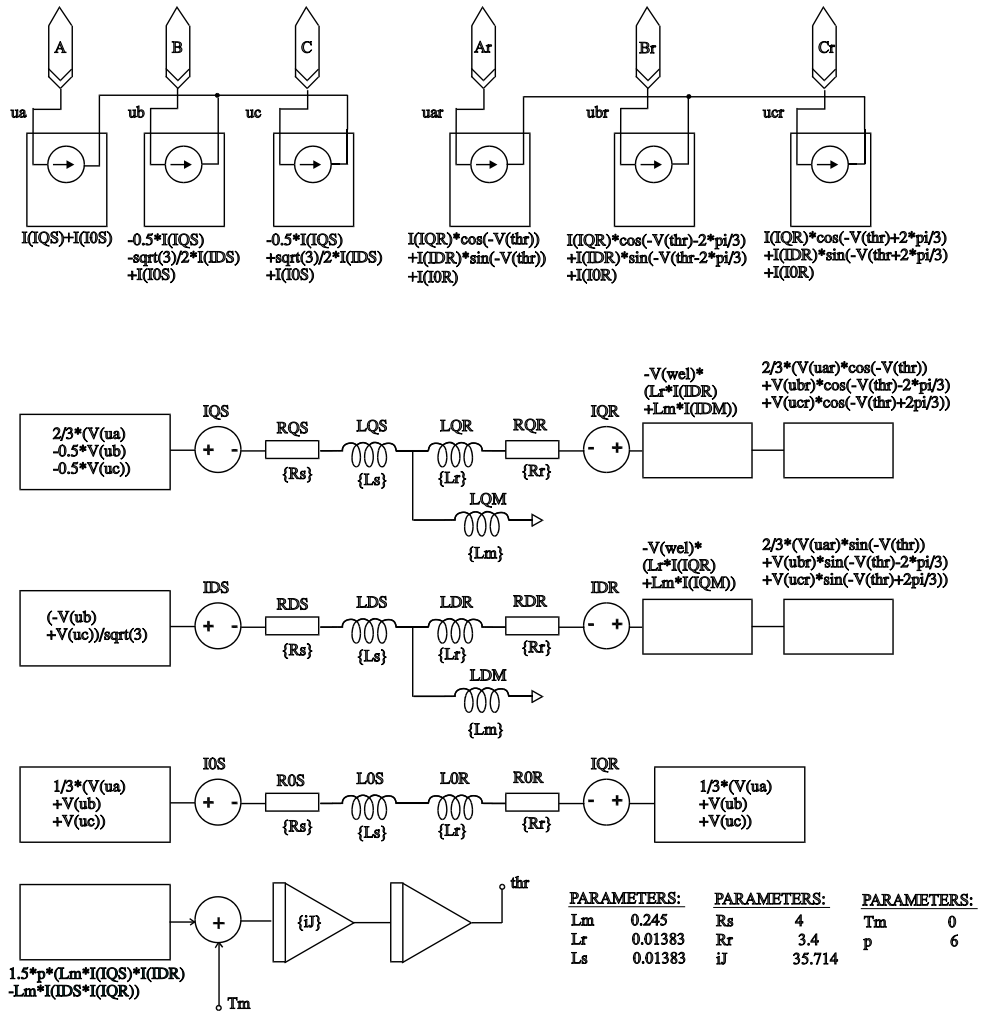

Fig.2 Induction motor model for PSPICE

where $V(ua)$ is the voltage of the node *ua*, $V(ub)$ is voltage of the node *ub* and $V(uc)$ is the voltage of the node *uc*.
The stator *qd0*-axis current is measured by the zero voltage source *IQS*, *IDS* and *I0S*. The notation $I(IQS)$ is for the current through *IQS*, $I(IDS)$ is for current through *IDS* and $I(I0S)$ for current through *I0S*.

Stator *qd0* axis resistance are *RQS*, *RDS* and *R0S* respectively. These parameters have same numerical value {*Rs*}. The stator *qd0* leakage inductance *LQS*, *LDS* and *L0S* have the same value {*Ls*} given as a parameter. In the similar manner magnetising inductanes *LQM* and *LDM* have the same numerical value {*Lm*}. The *q*-axis magnetising current is measured by *IQM* and the *d*-axis magnetising current is measured by *IDM*.

In the similar manner, rotor side voltage can be presented by appropriate ABM blocks. *qd0* resistances and rotor leakage inductance have the same value {*Rr*} and {*Lr*}. The rotor *qd0*-axis currents are measured by *IQR*, *IDR* and *I0R*.

The *q* and *d*-axis rotational voltages are presented by ABM blocks. Output voltage for q-axis is expressed by:

$$-V(wel)*(Lr*I(IDR)+Lm*I(IDM)),$$

and for d-axis by:

$$-V(wel)*(Lr*I(IQR)+Lm*I(IQM)),$$

according to Eqs. (17) and (18). $V(wel)$ is the voltage of the node *we* corresponding electrical angular speed.

The electric torque T_e is calculated by an ABM block. Its output voltage is determined by expression:

$$1.5*p*(Lm*I(IQS)*I(IDR)-Lm*I(IDS)*I(IQR))$$

according to Eq. (20). The voltage in node T_m is the applied mechanical torque (1Nm=1V). The rotor electrical angular velocity is solved by an integration block. Its input is the sum of the electric and mechanical torques. The gain of integration block $1/J$ is given as a parameter *iJ* [1/kgm^2].

The rotor position angle that is necessary for the rotor voltage transformation is obtained by the rotor speed integration.

The three phase stator currents are derived from stator *qd0*-axis currents by using inverse axis transformation from Eq. (1). The current sources connected to nodes *ua*, *ub* and *uc* fullfill these equations. The three phase rotor currents are obtained in the similar manner applying the rotor transformation given in Eq. (2).

IV. Simulation Result

To study start-up induction motor dynamic using PSPICE, a symmetrical three phase induction motor is considered. The parameters of the machine are given in Table 1. Core losses and mechanical losses are neglected.

The induction machine variables during free acceleration are shown if Fig. 2-4. The machine is initially stalled when rated balanced voltage is applied.

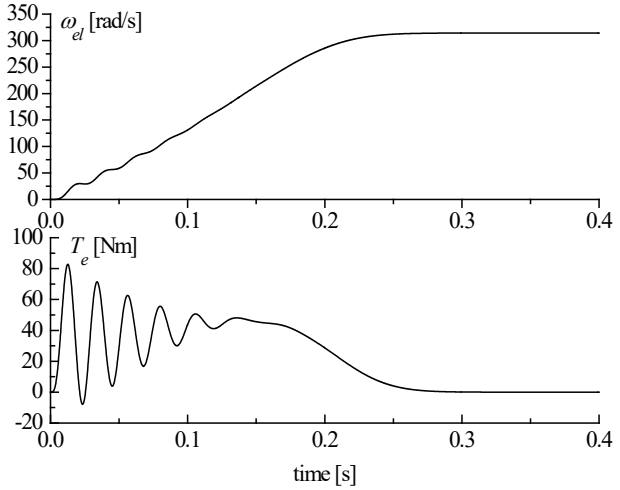

Fig.3. Speed and electric torque during free acceleration

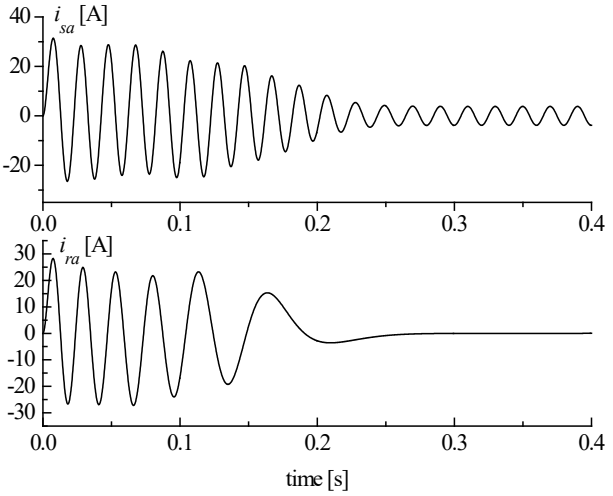

Fig.4. Stator and rotor current during free acceleration

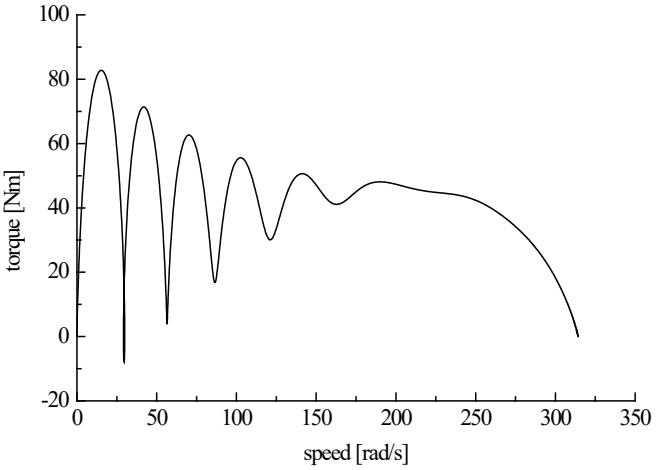

Fig.5. Torque-speed characteristics

The results are in close agreement with [1, 4].

TABLE I.
Motor data

P=4 kW;U_n=380 V; I_n=4 A		
L_{lr}=0.01383 H	L_{ls}=0.01383 H	L_m=0.245 H
r_s=4 Ω	r_r=3.4 Ω	p=6

V. Conclusion

As a software package PSPICE provides a simulation environment in which the design and application engineer can investigate practical drive system problems which may be encountered at the development stage or in an existing installation.

Presented model of the induction motor enables one simple model forming based on the equivalent scheme in *qd0* reference frame. Represented induction motor model contains the available electrical connections on the stator and rotor side so the motor coupling to feeding source is easy without regard is it power distribution network or power converter. Also, shown model can be applied for the analysis of single fed and double fed induction motor.

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Pspice Simulation of Power Electronics and Induction Motor Drives

Bojan Banković, Nebojša Mitrović, Vojkan Kostić, Milutin Petronijević

Abstract- Possibility of the PSPICE software package application on simulation of complex electromechanical systems is presented in this paper. The system considered is composed of two various subsystems, static semiconductor frequency converter - inverter and electrical motor. Validity of the proposed computer simulation concept is confirmed on the model of induction motor open loop variable speed drive supplied by square wave and PWM voltage inverter.

Keywords - variable frequency drive, PWM inverter

I. INTRODUCTION

In computer simulation of complex electromechanical system as variable speed drives with static power converter, in dependence of the goal and assignment the various methods exist, leading to the usage of different program packages. When the purpose of the analysis is concetrated on the power converter, CAD (Computer Aided Design) program packages for electrical circuit simulation like SPICE, ECAP etc. are used [1, 2]. The main characteristic of such models is that motor model is highly simplified and represented as RL circuit with electromotive force. If attention is directed toward electric machine program package based on the computer representation of the electric drive mathematical model, like SIMULINK, VISSIM etc. are used [3, 4]. This method is based on the idealization of the power source.

In this paper the system which consist of the induction motor - square wave (SQ) inverter and induction motor - pulse width modulation (PWM) inverter are simulated using PSPICE. The advantage of PSPICE application is the simple way of modelling the inverter, its switching, control and snubber circuits.

II. SYSTEM MODEL

The system considered is composed of two subsystems, static semiconductor frequency converter - inverter and induction motor.

The behaviour of the induction motor is analyzed on the basis of dynamical model. The classical rotating field theory with well-known *qd0* transformation is used [5].

The mathematical model in stationary reference frame is presented by Eqs. (1)-(3).

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$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ v_{qr} \\ v_{dr} \end{bmatrix} = \begin{bmatrix} R_s + sL_s & 0 & sL_m & 0 \\ 0 & R_s + sL_s & 0 & sL_s \\ sL_m & -\omega_r L_m & R_r + sL_r & -\omega_r L_r \\ \omega_r L_m & sL_m & \omega_r L_r & R_r + sL_r \end{bmatrix} \begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{qr} \\ i_{dr} \end{bmatrix} \quad (1)$$

$$T_e - T_m = J \frac{d\omega_r}{dt} \quad (2)$$

$$T_e = \frac{3}{2}\left(\frac{p}{2}\right) L_m \left(i_{qs} i_{dr} - i_{ds} i_{qr}\right) \quad (3)$$

The inverter is modelled on the basis of scheme in Fig. 1. The switching components are modelled as ideal voltage switches with RC snubber circuit. The fundamental frequency harmonic of the inverter output voltage is controled by means of appropriate control logic. A dc circuit is presented by three phase diode rectifier and appropriate LC filter. The control logic enables continual rise of the voltage along the defined *V/f* characteristic limiting in that way starting current.

The characteristic of the SQ inverter is that every half bridge unit alternates between ON and OFF state, Fig.3.

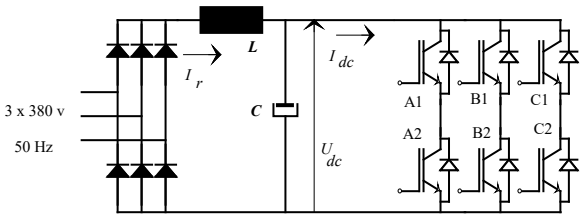

Fig 1. Three phase voltage source inverter

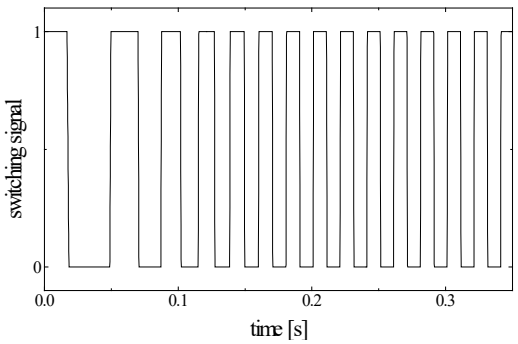

Fig. 3. Control impulses for switche A1

PWM inverter switches are controled by modulation signal shown in Fig. 2a. The modulation signal is generated with the purpose of the motor soft-start realization. The way in which the control impulses are generated for one PWM inverter switch is shown in Fig. 2b [1].

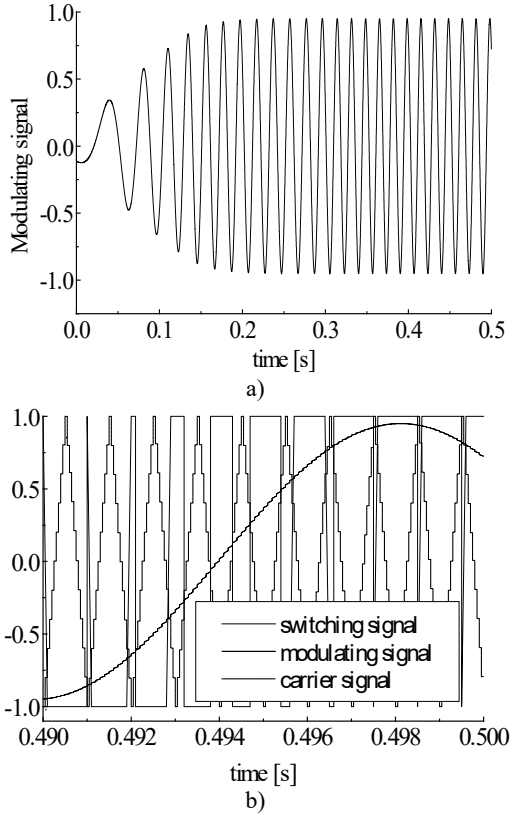

Fig.2a) Soft start modulation signal b) Generation of PWM signal

III. Inverter-Motor Coupling

Equivalent scheme of the system is chosen in order to enable simple connection of the motor and inverter. The ac power supply is modelled with three ideal voltage sources and the inverter load with three current sources with the currents equal to the phase motor currents. In that manner the influence of the induction motor on the inverter together with the load influence on the inverter dc link current are taken into account.

The complete equivalent scheme of the whole system is shown in Fig.4.

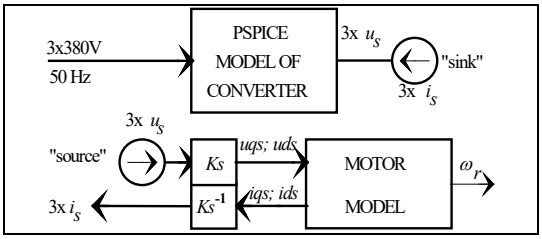

Fig. 4: Principle block diagram of system model

IV. Computer Simulation Result

Application of the described models in the PSPICE simulation package under different working conditions of the system induction motor-inverter have been simulated. The control logic have been designed in order to enable the well-known *V/f* regulation characteristic [5]. The behaviour of the system at the start of the induction motor with limited starting current have been simulated. The computer simulation results for PWM induction motor drive are shown in Fig. 5., and for SQ induction motor drive in Fig. 6.

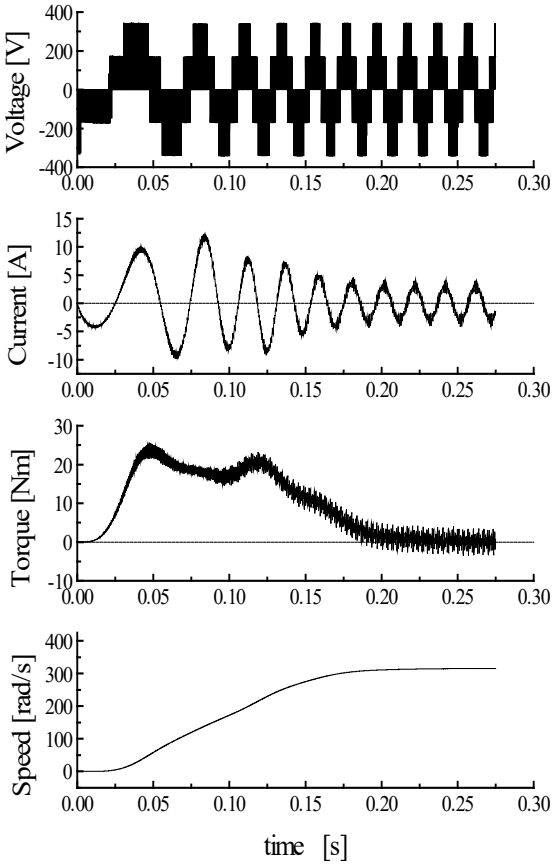

Fig. 5. Machine variable during free acceleration of PWM inverter induction motor drive

V. Experimental Model Verification

In order to verify the validity of the proposed concept experiment have been carried on the real PWM inverter fed drive in the Electric Drives Laboratory at the Faculty of Electronic Engineering in Nis.

Phase motor current, voltage and dc link current of the inverter for the frequency of the inverter carrier signal equal to 3.9 kHz are shown on Fig. 9-11.

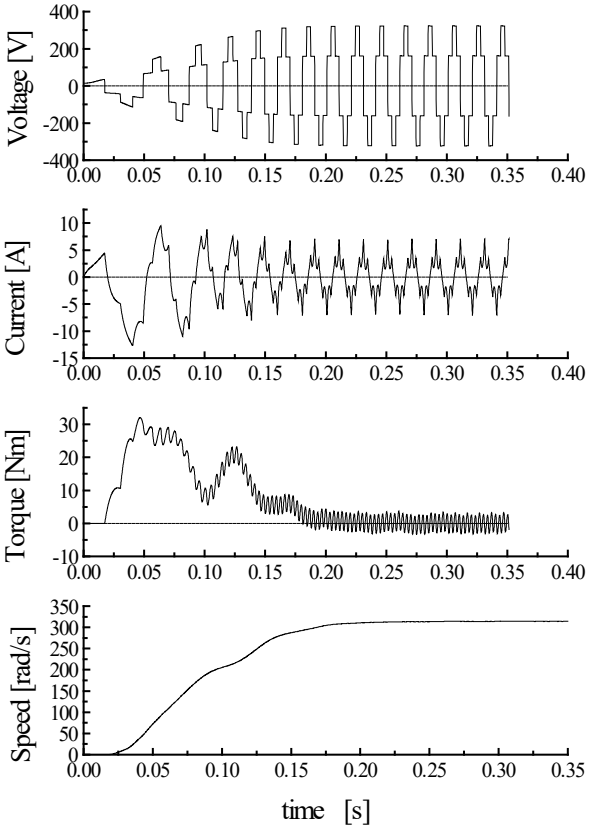

Fig. 6 Machine variable during free acceleration of SQ inverter induction motor drive

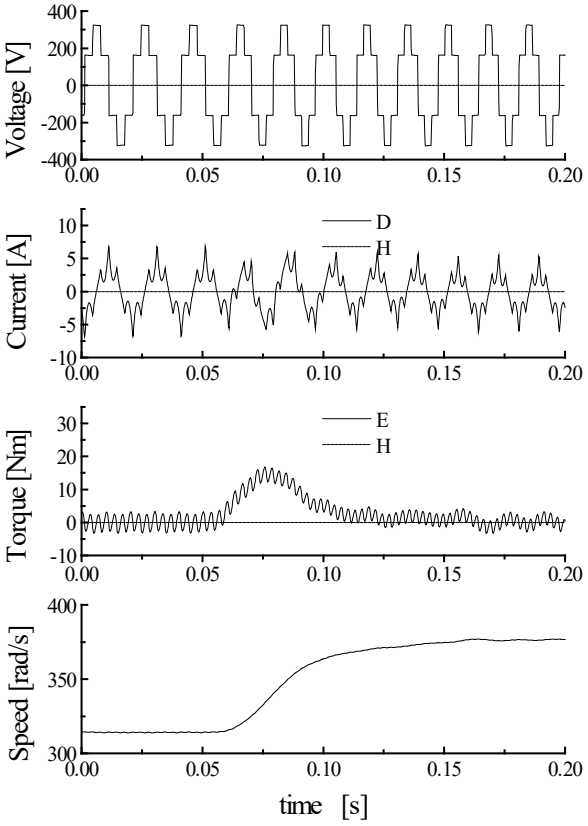

Fig. 8. Performance of a SQ inverter induction motor drive for a step change in inverter frequency

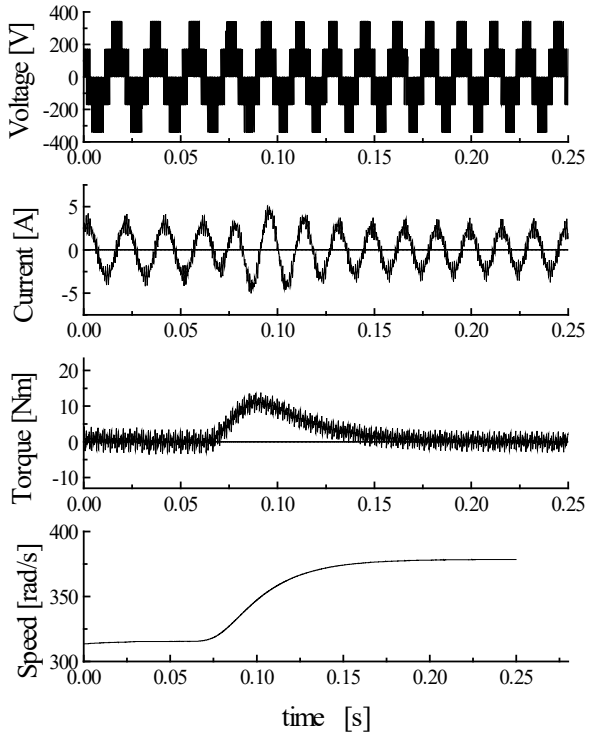

Fig. 7. Performance of a PWM inverter induction motor drive for a step change in inverter frequency

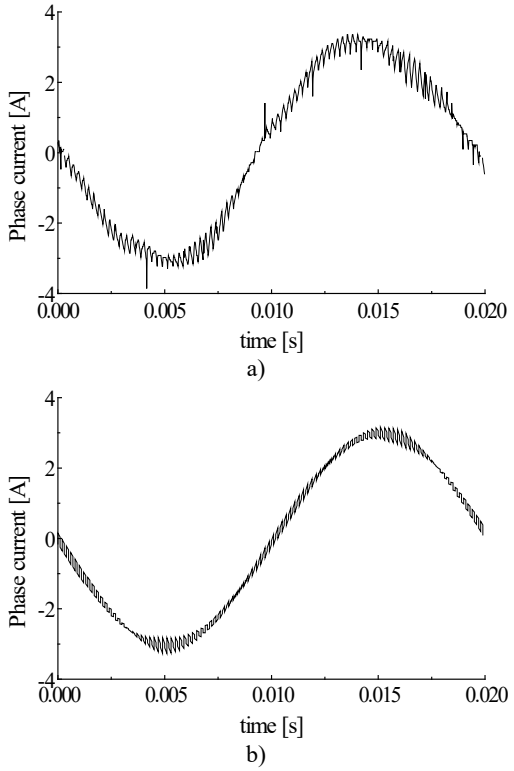

Fig.9. Motor phase current a) experiment b) model

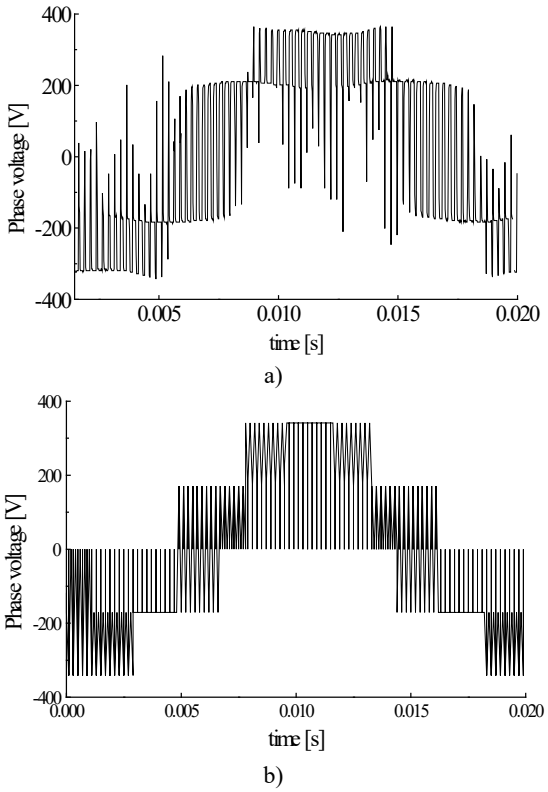

Fig.10. Motor phase voltage a) experiment b) model

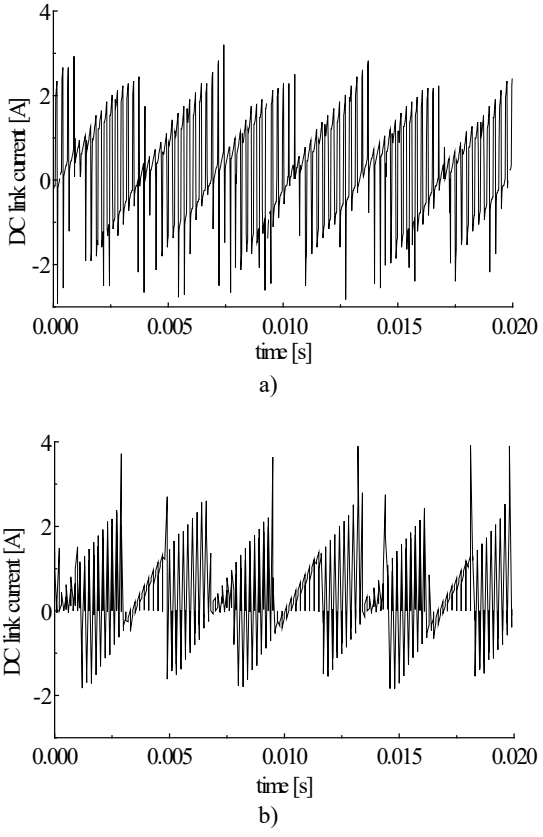

Fig.11. Inverter DC link current a) experiment b) model

VI. CONCLUSION

The application of CAD package like PSPICE admits efficient analysis of the behaviour of the different components of the modern variable speed drive. Described models and simulation results point out the important advantages of this concept in the modelling and analysis of the complex systems. This advantages are mainly based on adequate modelling of the interaction between electric machine and power converter. The proposed circuit topology is very closed to practical realization enabling in that way easy practical design and analysis of the complete system electrical machine-power converter.

Experimental verification of the proposed model confirmed our expected advantages of the proposed concept.

We would like to point out the possibility of analysing higher harmonic influence on the motor torque and influence of the inverter dead time.

New method for modelling of interaction between power electronic circuit and electric machine enables high flexibility in analysis and design. The main disadvantage of the proposed concept is the long simulation time conditioned by the extremely high ratio of the dominant time constants of the dynamical processes involved.

List of simbols:

v - instataneous voltage	i - instataneous current
T_e - electrical torque	ω_r - rotor speed
T_m - load torque	R_r - rotor resistance
L_m - magnetizing inductance	R_s - stator resistance
L_r - rotor inductance	J - inertia
L_s - stator inductance	s - diff. operator d/dt

- subscript:
a,*b*,*c* - phase quantities,
s- stator; r - rotor
d, *q* - direct and quadrature axis

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Vehicle Modelling Using Physical Networks

Milan Simić

Abstract - This paper presents a contribution in vehicle modelling that could be used in investigation and search for flat ride and beter passangers' comfort. Modelling approach, given here, is based on physical networks, i.e. analogies among various physical systems, in this case mechanical and electrical. Vibrations around pitch axis are anaylised and a novel model designed for simulations. Presented modelling method could be used for mechanical design improvements, for smart, active, suspension systems' design, or other applications, like energy recovery and harvesting in hybrid, or electrical vehicles.

Keywords - Physical networks, Smart suspension, Flat ride, Passenger comfort, Vehicle vibrations, Vehicle dynamics, Suspension design, Energy recovery.

I. Introduction

A moving vehicle is subjected to motion and vibrations along three axes: roll, yaw and pitch. It is happening regardless of the environment, i.e. it affects ground, air, water and underwater vehicles. Subjects of this study are ground vehicles performing translator motion and vibrations induced around pitch axis as shown in Fig. 1.

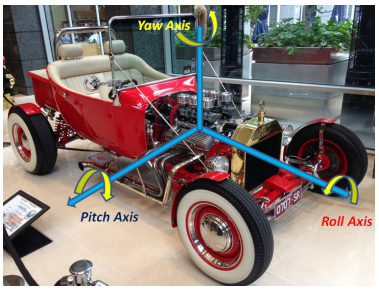

Fig. 1. Axes and vibration directions acting on a vehicle when performing translatory motion

An ordinary car, with four wheels, as a complex mobile system, if often presented using simplified, two-wheel bicycle model. This representation is used for vibration studies and flat ride investigations, as shown in [1], as well as for the path planning of the autonomous vehicles to achive the maximum ride comfort [2]. It is also used for autodriver algorithm development [3, 4]. Depending on the application, different views and parameters of the bicycle model are considered. Further simplification, used in vibration studies, is to *decouple* that car bicycle model.

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Following that, we assume that the front wheel excitation does not affect subsystem at the rear axle and vice versa.

By using *physical networks* approach it is possible to conduct more comprehensive vibration studies while taking into account mutual influences from forces acting on front or rear axles. Physical networks express amusing analogies of ordinary differential equations used to represent various physical and engineering systems. More on those modelling solutions could be found in [5-7].

II. Bicycle Model

Bicycle model used in this investigation is given in Fig. 2. Vehicle is represented as a beam of mass m, equally distributed along the length $l=a_1+a_2$ and with a moment of inertia I. It is a two degree-of-freedom (DOF) system where mass center is located in C and it is centre of rotation, i.e. bounce and pitch motion, with angular speed of w and angle Θ. Interfacing to mechanical translational reference, i.e. road, is realised by two sets of springs, K_f, K_r, and friction elements, B_f, B_r. We will investigate car body upward velocities (v_f, v_c, v_r) and displacements (x_f, x_c, x_r) along x axes.

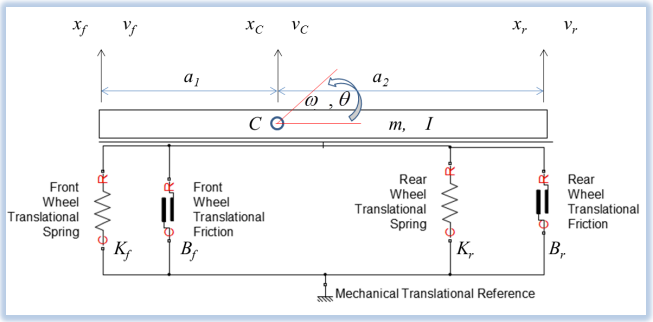

Fig. 2. Model 1: The bicycle model of a car as a beam of mass m and moment of inertia I, sitting on two sets of springs and friction elements representing two wheels

The translational coordinate x_C and the rotational coordinate θ are the usual generalized coordinates used to measure beam kinematics. Driving over the bumps on the road generates vertical forces that are acting on the two sides of the vehicle body, i.e. mass beam as shown in the Fig. 2. That action causes rotation represented by an angle θ. Moment of inertia of a beam with mass m is given as shown in Eq. (1):

$$I = \frac{1}{12} m l^2 \tag{1}$$

Radius of the beam rotation is given by Eq. (2):

$$R = \sqrt{\frac{I}{m}} \tag{2}$$

Vehicle on the road is subject to vertical forces acting on the front, F_f, and rear axle, F_r. We can add them, as they act together, in reference to the total body mass centre as given by Eq. (3):

$$F_f + F_r = m\frac{dv_C}{dt} \tag{3}$$

Adding moments of inertia, in reference to the mass centre, is presented by Eq. (4):

$$I\frac{dw}{dt} = mR^2\frac{dw}{dt} = F_r a_2 - F_f a_1 \tag{4}$$

Totall mass of the vehicle, as shown in Fig. 2, can be seen as two masses that correspond to the front, m_f, and the rear, m_r, part of the body, together with a *mutual mass, m_m,* between them, as given in the Fig. 3. Forces acting on the front and rear end of the vehicle are shown in the figure as ideal force sources. Mutual mass express influences of the forces acting on one part of the vehicle to the other and vice versa.

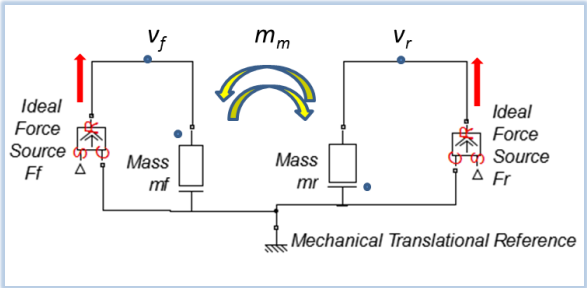

Fig. 3. Model 2: Mass represented as a coupled element

As it is show in [6], all three masses can be easily determined through calculations given by the set of equations Eq. (5-7):

$$m_f = m\frac{a_2^2 + R^2}{l^2} \tag{5}$$

$$m_r = m\frac{a_1^2 + R^2}{l^2} \tag{6}$$

$$m_m = m\frac{a_1 a_2 - R^2}{l^2} \tag{7}$$

From the Eq.(7) we can see that the decoupling condition is when m_m=0. It is given as expression in Eq. (8). In that case and we can treat parts of the vehicle's body separately.

$$R^2 = a_1 a_2 \tag{8}$$

Finally, we can write equations of motion as following:

$$m_f\frac{dv_f}{dt} + m_m\frac{dv_r}{dt} = F_f \tag{9}$$

$$m_m\frac{dv_f}{dt} + m_r\frac{dv_r}{dt} = F_r \tag{10}$$

These equations correspond to the mechanical systems diagram, or physical network, as shown in Fig. 3. The polarities of the mutual mass influences are given by dots. As in any other coupled physical network, polarities depend on the defined positive direction on the diagram.

III. Physical Networks

Physical network represents a class of linear graph associated to the particular physical system equations. Basic definitions, principles and rules for solving system equations, represented by the network, are independent of physical system. In a physical network there are two basic time dependent variables: flow, *f*, and potential, *p*. Flow is a variable that streams through network elements and connection lines, while potential is a variable manifested and measured across network elements, between two network points. Potential of a point in the network depends on the chosen referent point.

Examples of physical variables are electrical *current* and *potential*. Current is directly related to the mechanical motion of the electrical charges. Potential difference is called voltage. We have *force* and *velocity* in a mechanical system with translation, or *torque* and *angular speed* in a mechanical system with rotation. There are *flow* and *pressure* in hydraulic systems. Modelling of various systems can be implemented using the same type of ordinary differential equations (ODE), or physical network diagrams. Comparing electrical and mechanical system with translation, we can see analogies as given in Table I.

TABLE I
Electrical / Mechanical Analogies

Relation \ System	Electrical	Translation
Proportion	$i = \frac{1}{R}u$	$F = Bv$
Integration	$i = \frac{1}{L}\int udt$	$F = K\int vdt$
Differentiation	$i = C\frac{du}{dt}$	$F = m\frac{dv}{dt}$

IV. System Modelling Steps

In this section we will perform modelling of the vehicle together with the road conditions and their interaction. The scenario is shown in Fig. 4. Vehicle is riding over the road bump. That will cause pitch motion, which should fade into the bounce motion, as quick as possible, for the comfortable flat ride. Road imperfection will generate two upward forces acting on front and then on the rear axle delayed in time. Time delay is defined by the translatory speed of the vehicle.

Fig. 4. Riding over a bump on the road

Road bumps can have various shapes, high and lengths. Sometimes step, or pulse functions could be used, as in flat ride studies and design [1]. In our case, as shown in Fig. 4, we are dealing with a harmonic type road bump with the amplitude of A=0.05m and the length of 1m.

Kinodinamic characteristics of the vehicle are given as following:

- Vehicle mass is m=1500,
- the length is l=4m,
- front and rear interfacing springs are the same and equal to K_f=K_r=2000N/m,
- while friction components are also the same and have value of B_f=B_r=10.

Translatory speed of the vehicle is v_t=10m/s.

We will assume that the centre of the mass is in the middle of the beam. Following that, the radius of rotation can be found using equations Eq. (1) and Eq. (2). It is equal to $R = \frac{2\sqrt{3}}{3}$. Using equations Eq. (5-7) values for the masses m_f, m_m, m_r are calculated and presented in Eq. (11).

$$\begin{aligned} m_r &= m_r = 500 \\ m_m &= 250 \end{aligned} \tag{11}$$

Through the whole document MKS units are used, unless otherwise specified. Vehicle model that corresponds to this case is given in Fig. 3, while motion equations are specified by Eq. (9) and Eq. (10). For the simplicity of the modelling process we will now transfer our system into and electrical circuit as given in Fig. 5.

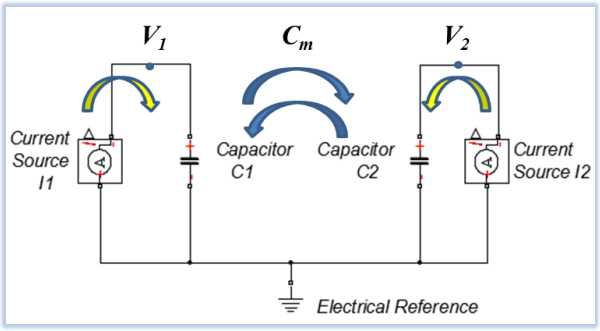

Fig. 5. Model 3: Vehicle model as an electrical network, where current corresponds to force and voltage to velocity

We can now write equations of motion, converted to electrical circuit, as following:

$$C_1 \frac{dv_1}{dt} + C_m \frac{dv_2}{dt} = I_1 \tag{12}$$

$$C_m \frac{dv_1}{dt} + C_2 \frac{dv_2}{dt} = I_2 \tag{13}$$

Further model transformation is to simplify it as shown in the Fig. 6. We can now write system equations and establish correspondence between two circuits.

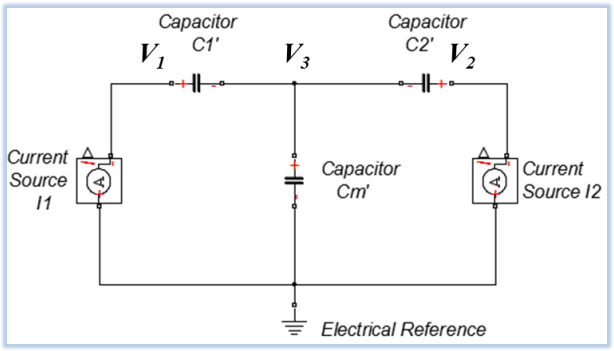

Fig. 6. Model 4: Simplified electrical network

Following equations are related to model 4:

$$C_1'\left(\frac{dv_1}{dt} - \frac{dv_3}{dt}\right) = I_1 \tag{14}$$

$$C_2'\left(\frac{dv_2}{dt} - \frac{dv_3}{dt}\right) = I_2 \tag{15}$$

$$C_m' \frac{dv_3}{dt} = I_1 + I_2 \tag{16}$$

By comparing equations Eq. (12) and (13) with equations set of Eq. (14) to (16) we can derive expressions for model 4 circuit elements $C_1', C_2' \text{ and } C_m'$. Finally, when we put numerical values for our particular system we can get the following:

$$C_1^{'} = C_2^{'} = 250$$
$$C_m^{'} = -750 \quad (17)$$

By looking at the Table I we can see that the mass corresponds to capacity, spring stiffness to inductivity and friction to resistivity. When MKS used there is direct correspondence between units for physical quantities in various physical network systems. This means that if mass is expressed in *kg*, then the corresponding capacity will be expressed in *F*. Beam of mass m=1500kg, from the bicycle model as given in Fig. 2, is represented by model 6 where capacitor values are given by Eq. (17) in Farads.

V. Comprehensive Model

In previous section we have performed modelling of the vehicle body including effects of the mutual interferences between vertical motions caused by the forces acting one axle of the vehicle to the whole body. In the following section we will include interfacing between body and the road. We will refer to the whole bicycle model as shown in Fig. 2. Since vehicle body representation, given by model 4, is now an electrical circuit, we will convert the whole system to electrical. Model 5 is shown in Fig. 7.

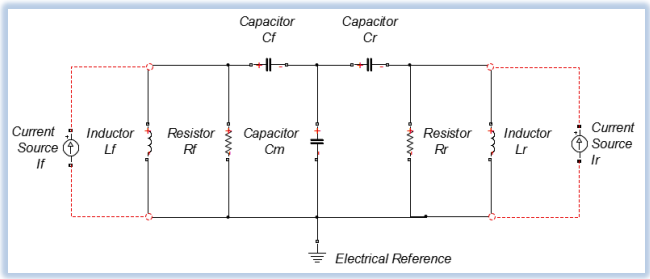

Fig. 7. Model 5: Electrical circuit as a representation for the vehicle bicycle model shown in Fig. 2

In Fig. 7 set of capacitors represent mass of the vehicle body, from model 4, while resistors and inductors correspond to the wheels parameters, i.e. friction and stiffness interfacing components to that road. Road is represented by electrical ground. Models 1-5 are not functional models. They are just used to demonstrate steps and principles in whole system design. Models, that follow in this report, are full functional models, running in Simulink environment, based on MATLAB R2012b.

Riding over the road bumps is an isolated event, i.e. two linked events: bump under the front wheels and then, after a delay, bump under the rear wheels. That causes vertical forces on front and rear axle of the car. We can model force sources as controlled current sources. Road bump of amplitude A will generate force F given by the Hooke's law:

$$F = kx = KA \quad (18)$$

Since the bump follows a harmonic waveform we need to find its period, i.e. the frequency, to be able to perform modelling. Since the velocity of the horizontal translator motion is equal to v=10m/s travelling time over the bump is 0.1s, which is the half of the sinusoidal signal period. So we have T=0.2s and f=5Hz. Our force sources are positive half-periods of the waveform as given by Eq. (19).

$$F = kx\sin(2\pi f) = 1000\sin(10\pi) \quad (19)$$

We have K=k=20000N/m and x=A=0.05m. Simulink model of the force source F_f is given in the Fig. 8.

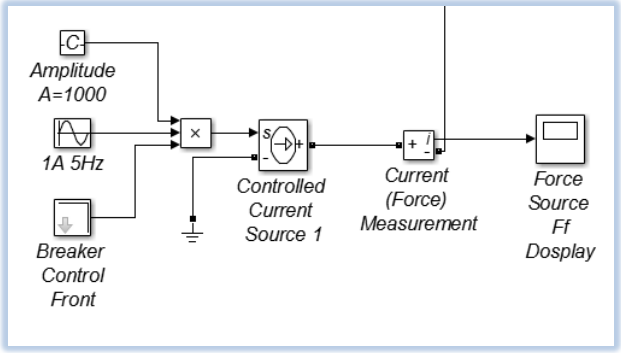

Fig. 8. Simulation of the force source generated by the road bump acting on front wheels

Model for the force source acting on the rear wheels is the same, but with a delay implemented. Delay depends on the vehicle speed. Force sources F_f and F_r graphs are given in Fig. 9 and Fig. 10 respectively

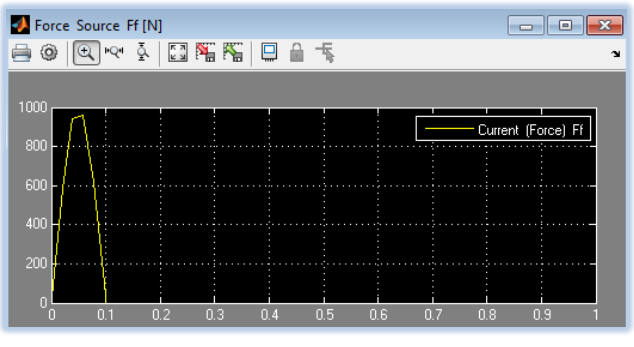

Fig. 9. Vertical force F_f generated by a bump on the road. Axes x represent time in *sec*.

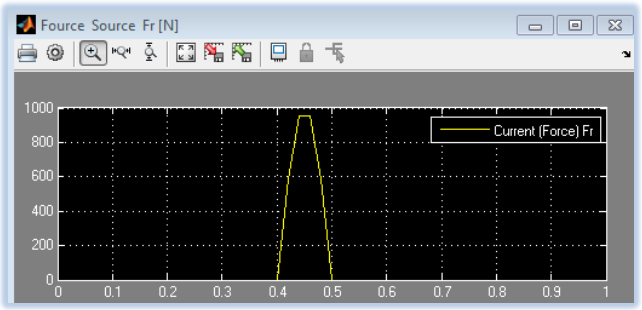

Fig. 10. Vertical force F_r generated by a bump on the road. Axes x represents time in *sec*.

Complete model of the vehicle on the road, including the scenario of the ride over the road bump, is given in Fig. 15. In addition to vehicle system components, already described and explained comprehensively, measurement and display devices are shown. For example, since vertical displacement is integral of the vertical velocity a circuit for integration is added, consisting of capacitor with the value C=1. Front vertical velocity is shown in Fig 11, while all displacements are presented in Fig 12.

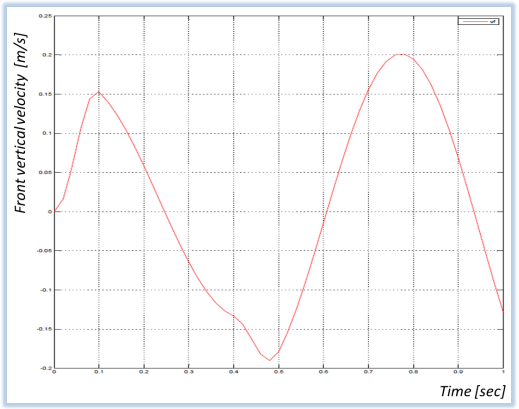

Fig. 11. Front vertical velocity generated by a bump on the road expressed in *m/s*. Axes x represents time in *sec*.

From the Fig. 12 we can see that the *front* is first going up, while the *back* end is going down. This is the result of the mutual mass interaction and can be observed in the real life scenario. At the same time mass centre is exposed to the minim disruption, which is contributing to the ride comfort when the passenger is sitting close to it.

In addition to the research capabilities opened by this modelling approach, in the areas of *flat ride* and *smart suspension* design, this model can be used for the green energy, or energy recovery investigation. Solar and thermal energy harvesting, for the automotive applications, are already subjects of intensive research, but recovery of the kinetic energy dissipated while driving over the bumpy road, could be subject to another interesting study.

Instant power in mechanical systems is product of force and velocity. Powers from the front and from the back of the vehicle are calculated and shown in Fig. 13.

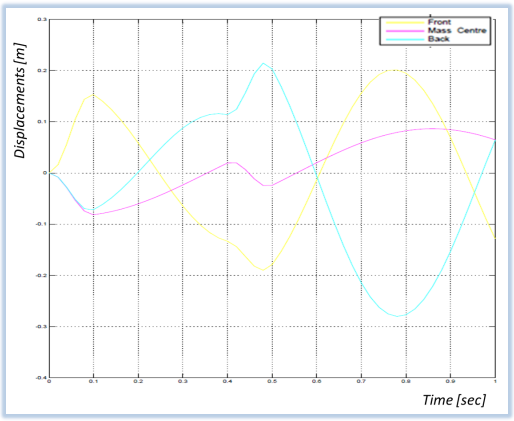

Fig. 12. Displacements from the three key body points: front, centre of mass and back of the vehicle

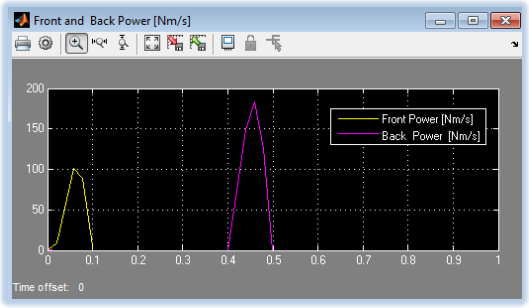

Fig. 13. Study of power dissipation. Axes x represents time in *sec*.

V. Experimental Testing

Analytical, as well as, simulation and modelling investigations in vehicle vibrations, are accompanied by lab experiments. RMIT University School of Engineering vibration lab is shown in Fig. 14. The whole lab setup was conducted by students and it is subject to constant improvements so that more comprehensive research can take place. One of the next steps is implementation of the hardware in the loop testing and smart suspension.

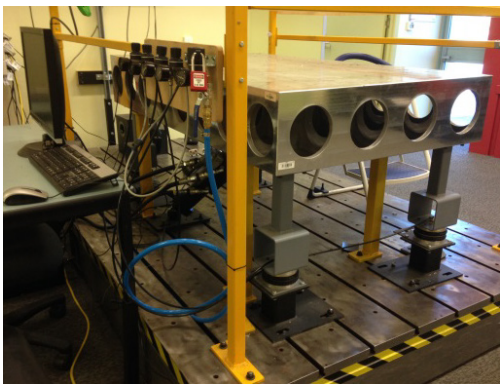

Fig. 14. Vehicle vibration lab at RMIT University

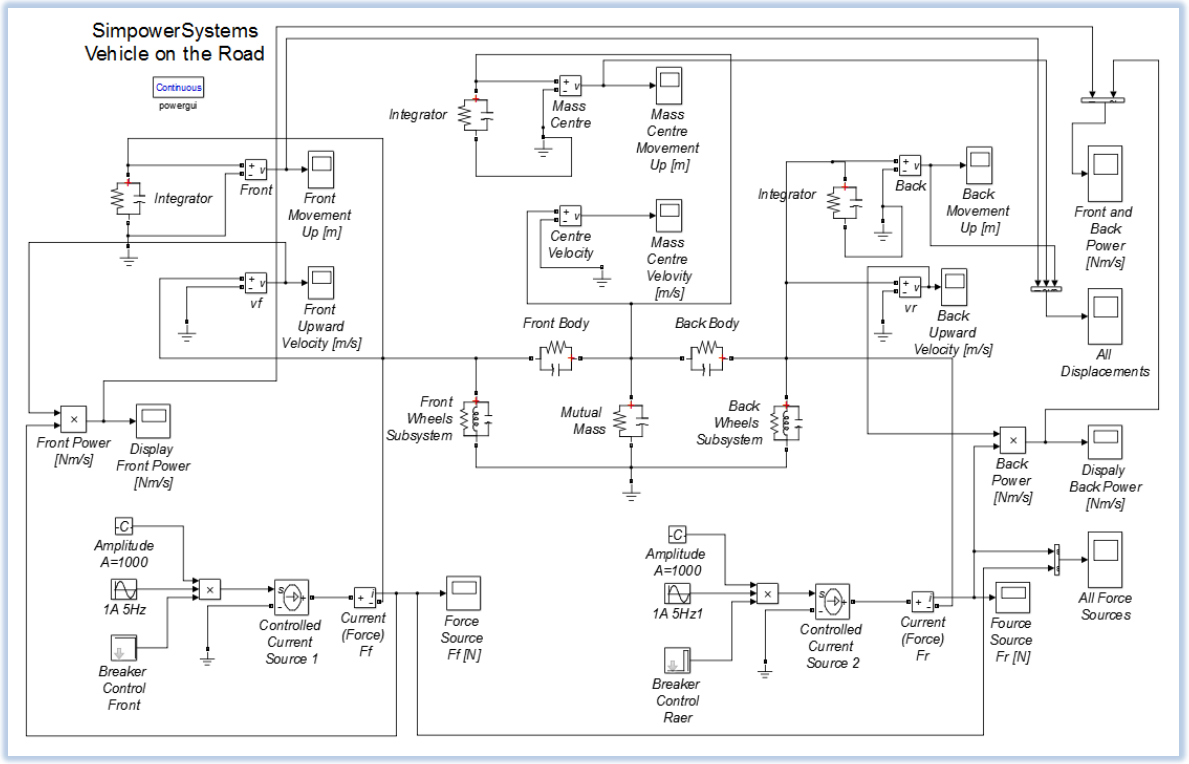

Fig. 15. Simulink model of the vehicle on the road

VI. Conclusion

In this paper a novel modelling of a vehicle and its road interaction is presented. It is based on physical networks and analogies between electrical and mechanical systems. There is a wide range of possible applications. We could investigate vehicle vibrations and ride comfort. In addition to that we could analyse other system quantities and parameters. Forces, power and energy could easily be monitored. Further applications of the model will be in the hardware in the loop testing for the research in smart suspensions.

Acknowledgement

I would like to acknowledge Professor Vančo Litovski for introducing me to this amusing area of physical networks.

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Small Signal Modeling of Series-Parallel Resonant Converters Based on Extended Describing Function

Milan Pajnić, Miroslav Lazić, Zoran Cvejić

Abstract - In this paper small signal modeling of series-parallel resonant converters based on extended describing function is presented. Resonant equivalent circuit state variables are approximated by their fundamental harmonics. By using extended describing function method and with separation of state variables, state space model of resonant converter is obtained. Small-signal model is analyzed in two main operation modes, when switching frequency is bellow and above frequency of resonant tank. Movement of zeros and poles of small signal model is presented in respect operation mode and ratio between switching and resonant frequency.

Keywords – Resonant converter, LLC converter, extended describing function, small-signal model.

I. INTRODUCTION

The resonant converters have advantages for high power or high-frequency power conversion. [1] Series or parallel resonant converters suffer from several drawbacks that limit its usefulness in many applications. Series resonant converters have small variation of dc conversion ratio over large range of switching frequency and are incapable of regulating output voltage when unloaded. In some applications, at light loads, the resonant current is reduced to a point where zero-voltage switching (ZVS) is lost.

These drawbacks are avoided with development of parallel, series-parallel, and many other higher-order resonant topologies [2]. The LLC series resonant converter (LLC- Series-parallel converter fig. 1) modifies the gain characteristics of a series resonant converter (SRC) and improves the light-load efficiency allowing boost mode operation.

Analysis methodologies that have been developed for modeling small-signal dynamics of power converters can be classified into two main categories. Averaging technique starts from state space description of each topology. It applies small ripple approximation and average time-invariant model is derived. After linearization and neglecting higher order terms, *s* domain transfer functions are obtained. *State space average* method has been used for converters with PWM regulation to analyze small signal dynamics, and provides accurate method for up to half switching frequency. The resonant converter switching frequency is close to resonant tank natural frequency, so states contains mainly switching frequency harmonics instead of low frequency content like in PWM converter. Since average method will eliminate the information of switching frequency, it cannot predict the dynamic performance of resonant converter.

For discrete modeling technique, state space system is also starting point. Equations are formed from equivalent circuit difference equations. However this method introduces error by approximation of transition in linear terms during one switching period.

The describing function concept has been introduced in [3]. The control-to-output and line-to-output describing functions are defined under the constant line voltage and constant control signal, respectively. Output control voltage is expressed as a Fourier series expansion. The resulting converter output voltage component at the same frequency as that of the perturbation signal is found by calculating the amplitude and phase of the fundamental term in the Fourier series. Extended describing function method proposed in [4] is a simplified modeling method based on description function method presented in [5]. Accuracy of this method has been verified in [6] based on analysis of series and parallel resonant converter. Detail small-signal characteristic of resonant LLC converter has been presented in [7] using simulation tool to emulate function of impedance analyzer to get the small signal response of resonant converter.

In Section II equivalent circuit of LLC converter is presented and extended describing function method is introduced. State space model is obtained with isolation of equation variables. Small-signal model characteristics of converter are presented in Section III. For a range of switching frequency two main modes have been identified and movement of zeros and poles presented. Section IV states the conclusions.

II. SMALL SIGNAL MODELING

The circuit diagram of an LCC resonant converter is shown in Fig. 1, and equivalent circuit is shown in Fig. 2.

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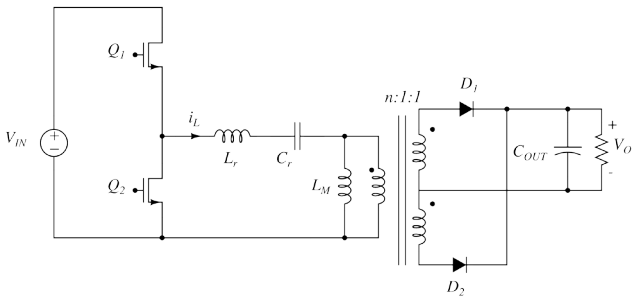

Fig. 1: Circuit diagram of an LCC resonant converter.

A. Nonlinear State Equation

The input voltage V_g is assumed to be symmetric square wave, with its magnitude proportional to the DC input voltage. The equivalent circuit provides the following nonlinear state space equations, where i_{L_r}, i_{L_M} and v_{C_r} are the state variables and V_O is the output variable:

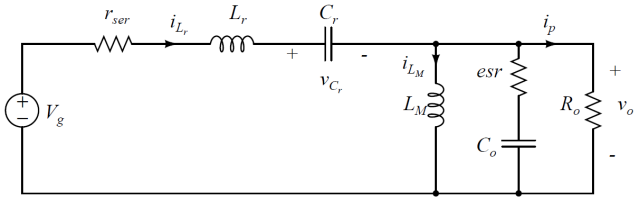

Fig. 2: Equivalent circuit diagram of LLC resonant converter

$$V_g = i_{L_r} r_{ser} + L_r \frac{di_{L_r}}{dt} + L_M \frac{di_{L_M}}{dt} + v_{C_r} \tag{1}$$

$$L_M \frac{di_{L_M}}{dt} = (i_{L_r} - i_{L_M}) R_O = \text{sgn}(i_{L_r} - i_{L_M}) V_O \tag{2}$$

$$\frac{dv_{C_r}}{dt} = \frac{i_L}{C_r} \tag{3}$$

In this implementation of resonant converter, the output voltage is regulated by modulating the switching frequency where the operating point is determined by $\{v_g, \omega_s, R_O\}$.

B. Harmonic Approximation

According to [8] typical waveforms of the variables shown in Fig.2 can be approximated by fundamental harmonics, and the output capacitor voltage can be approximated by its dc component. Referring to [7], when converter is operating in continuous conduction mode with higher order of harmonics took into consideration the model will not be improved significantly, which is understandable since in continuous conduction mode LLC is operating like SRC. When converter is operating in discontinuous conduction mode observing fundamental component is not enough. With more harmonics considered, the model will be different especially in frequencies near double beat pole [7].

By making this assumption, we have:

$$i_{L_r}(t) = i_{L_{rS}}(t)\sin(\omega_s t) + i_{L_{rC}}(t)\cos(\omega_s t), \tag{4}$$

$$i_{L_M}(t) = i_{L_{MS}}(t)\sin(\omega_s t) + i_{L_{MC}}(t)\cos(\omega_s t), \tag{5}$$

$$v_{L_r}(t) = v_{L_{rS}}(t)\sin(\omega_s t) + v_{L_{rC}}(t)\cos(\omega_s t), \tag{6}$$

where terms $\{i_{L_{rS}}, i_{L_{rC}}, i_{L_{MS}}, i_{L_{MC}}, v_{C_{rS}}, v_{C_{rC}}\}$ are slowly time varying components.

C. Extended Describing Function

By using the extended describing function method [6], the nonlinear terms in (1-3) can be approximated either by the fundamental components terms or by the DC terms to give:

$$V_g \approx \frac{4}{\pi}\sin(\pi d) V_g \sin(\omega_s t) \tag{7}$$

$$\text{sgn}(i_{L_r} - i_{L_M}) V_o = \frac{4}{\pi}\frac{i_{L_{rS}} - i_{L_{MS}}}{i_p} V_o \sin(\omega_s t) + \tag{8}$$

$$+ \frac{4}{\pi}\frac{i_{L_{rC}} - i_{L_{MC}}}{i_p} V_o \cos(\omega_s t)$$

$$\left| i_{L_r} - i_{L_M} \right| = \frac{2}{\pi} i_p \tag{9}$$

$$i_p = \sqrt{(i_{L_{rS}} - i_{L_{MS}})^2 + (i_{L_{rC}} - i_{L_{MC}})^2} \tag{10}$$

With the small-signal modulation frequency lower than the switching frequency, by substituting (4-10) into (l-3), and by equating the coefficients of dc, sine, and cosine terms respectively, we get:

$$\frac{4}{\pi}\sin(\pi d) V_g = i_{L_{rS}} + L_r (di_{L_{rS}}/dt - \omega_S i_{L_{rC}}) + v_{C_{rS}} + \tag{11}$$

$$+ L_M (di_{L_{MS}}/dt - \omega_S i_{L_{MC}})$$

$$0 = i_{L_{rC}} + L_r \left(\frac{di_{L_{rC}}}{dt} - \omega_S i_{L_{rS}}\right) + v_{C_{rC}} + L_M \left(\frac{di_{L_{MC}}}{dt} - \omega_S i_{L_{MS}}\right) \tag{12}$$

$$L_M \left(\frac{di_{L_{MS}}}{dt} - \omega_S i_{L_{MC}}\right) = \frac{4}{\pi}\frac{i_{L_{rS}} - i_{L_{MS}}}{i_p} V_o \tag{13}$$

$$L_M \left(\frac{di_{L_{MC}}}{dt} - \omega_S i_{L_{MS}}\right) = \frac{4}{\pi}\frac{i_{L_{rC}} - i_{L_{MC}}}{i_p} V_o \tag{14}$$

$$C_r \left(\frac{dv_{C_{rS}}}{dt} - \omega_S v_{C_{rC}}\right) = i_{L_{rS}} \tag{15}$$

$$C_r \left(\frac{dv_{C_{rC}}}{dt} - \omega_S v_{C_{rS}}\right) = i_{L_{rC}} \tag{16}$$

$$V_o = \frac{2}{\pi} i_p R_o \tag{17}$$

$$\frac{dV_{oc}}{dt} = -\frac{V_{OC}}{C_O R_O} + \frac{2 i_p}{\pi C_O} \tag{18}$$

Equation (11-18) represents modulation equation, a nonlinear large-signal model of the LLC power stage. Inputs of (11-18) $\{v_g, \omega_s, d, i_p\}$ are varying slower than the switching frequency and by substituting (13) into (11) we

get:

$$\frac{di_{L_{rS}}}{dt} = \omega i_{L_{rC}} - \frac{4}{\pi}\frac{V_o i_{L_{rC}}}{L_r i_p} - \frac{dv_{C_{rC}}}{L_r} + \frac{4}{\pi}\frac{\sin(\pi d)V_g}{L_r} - \frac{i_{L_{rS}}}{L_r} \quad (19)$$

For the small signal model to be presented in state space form, each state variable needs to be isolated in the equation and represented as the sum of the remaining variables. Since a ratio between state variables exists in (19) $i_{L_{rS}} / i_p$ where $i_p = \sqrt{(i_{L_{rS}} - i_{L_{MS}})^2 + (i_{L_{rC}} - i_{L_{MC}})^2}$ it is clear that this relationship of the state variables cannot be put into the states vector, therefore the ratio $i_{L_{rS}} / i_p$ is put into small signal form with the use of *Taylor Series* expansion. After expanding i_p, perturbing the large-signal model around the operating point $i_{L_{rS}} = I_{L_{rS}} + \tilde{i}_{L_{rS}}$ $i_{L_{rC}} = I_{L_{rC}} + \tilde{i}_{L_{rC}}$ $i_{L_{MS}} = I_{M_{rS}} + \tilde{i}_{L_{MS}}$ $i_{L_{MC}} = I_{M_{rC}} + \tilde{i}_{L_{MC}}$ and eliminating 2nd order small signal terms and DC constant terms, we get $\tilde{i}_{L_{rS}} / \tilde{i}_p$ in small signal form. Using previous algorithm same can be derived for $\tilde{i}_{L_{rC}} / \tilde{i}_p$, $\tilde{i}_{L_{MS}} / \tilde{i}_p$ and $\tilde{i}_{L_{MC}} / \tilde{i}_p$. After linearization around operating point and, model can be represented in state-space form as follows:

$$\frac{d\tilde{x}}{dt} = A\tilde{x} + B\tilde{u} \quad (20)$$

$$\tilde{y} = C\tilde{x} + D\tilde{u} \quad (21)$$

where:

$$x = \left[\tilde{i}_{L_{rS}}\ \tilde{i}_{L_{rC}}\ \tilde{i}_{L_{MS}}\ \tilde{i}_{L_{MC}}\ \tilde{v}_{L_{rS}}\ \tilde{v}_{L_{rC}}\ \tilde{v}_{CO}\right]^T \quad (22)$$

$$u = \left[\tilde{d}\ \tilde{\omega}\right]^T \quad (23)$$

$$y = \left[\tilde{v}_O\ \tilde{i}_p\right]^T \quad (24)$$

III. Small Signal Characteristic of LLC Resonant Converter

Small signal characteristic of LLC converter (fig. 1.) is analyzed based on previous model. The simulation is performed for different operation modes in switching frequency range of 68-110 kHz. With use of extended describing function method, when converter is operating in continuous conduction mode, for $F \le 1$, where F is ratio between resonant and switching frequency, small signal characteristic is shown in figure 3. The graph contains one beat frequency double pole, one pole and one ESR left half plane zero. While operating near resonant frequency, beat frequency double pole will move to lower frequency. When switching frequency at resonant frequency the beat frequency double pole will split and become two real poles, figure 4. Moving to higher switching frequency will cause a double pole at lower frequency. Output capacitor ESR will cause a fixed frequency left half plane zero.

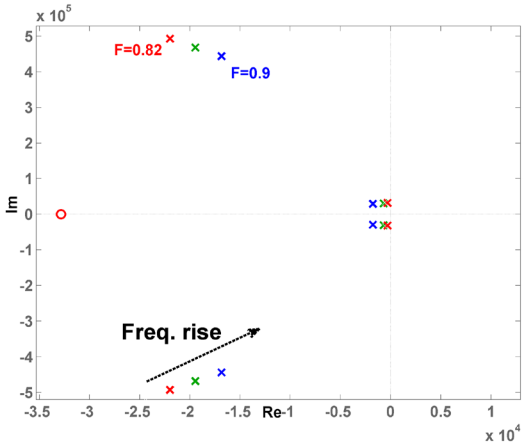

Fig. 3: Movement of poles and zeros for $F \le 1$ in CCM.

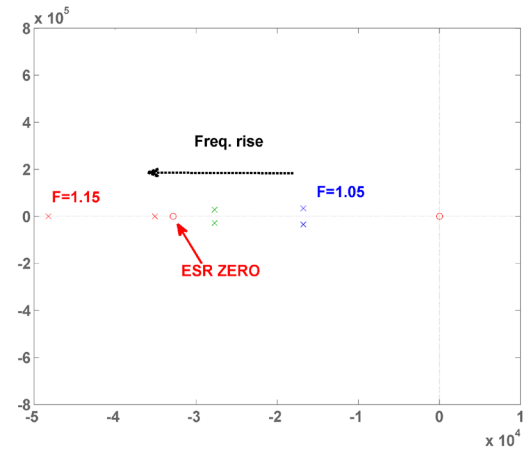

Fig. 4: Movement of poles and zeros for $F \approx 1$ in CCM.

When converter is operating in discontinuous mode, for $F \le 1$, small signal characteristic is shown in figure 5. In cases where switching frequency is lower than resonant frequency a right plane zero observable. In this case position of RHP zero is frequency dependent, but it doesn't shift to very low frequency even with F=0.8 or F=0.7.

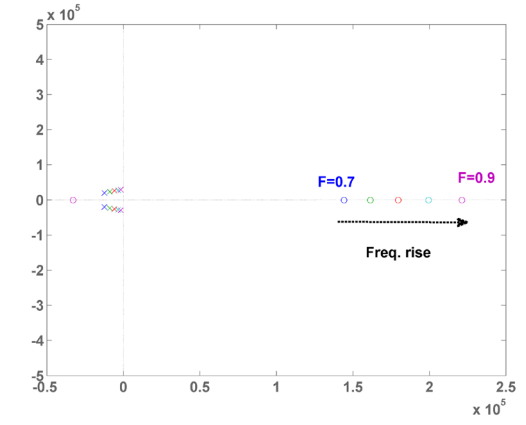

Fig. 5: Movement of poles and zeros for $F \le 1$ in DCM.

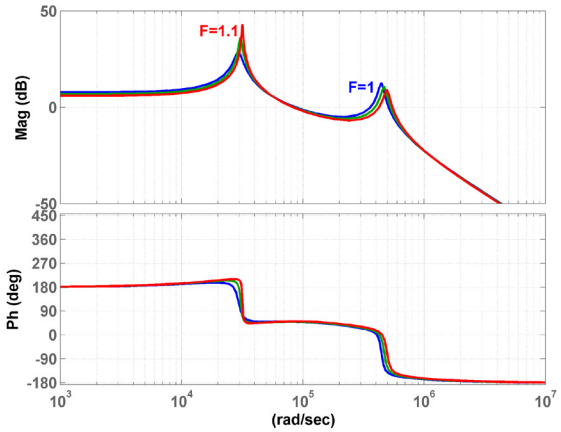

Fig. 5: Bode plot of control-to-output for CCM and $F \geq 1$.

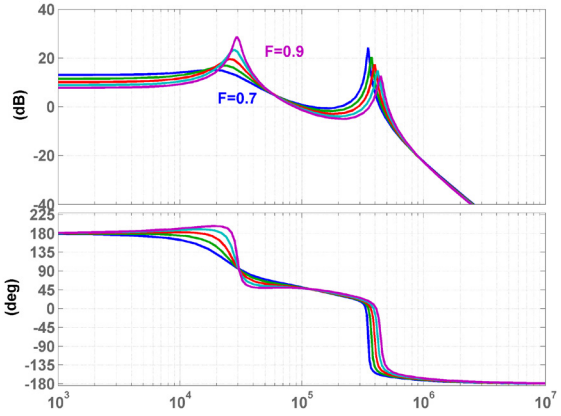

Fig. 6: Bode plot of control-to-output for DCM and $F \leq 1$.

In left half plane, referring to figure 5, there are two poles and one ESR zero. Compared to previous mode, poles they are less frequency dependent. Control to output transfer functions in different operation modes, CCM and DCM are presented in figure 5 and 6, respectively.

IV. Conclusion

In this paper a technique based on the extended-describing function was employed on modeling dynamics of LLC resonant converter. Resonant equivalent circuit state variables are approximated by their fundamental harmonics. To represent small signal model in state space form a separation of variables is performed with use of *Taylor Series* expansion. Movement of zeros and poles of small signal model is presented in respect operation mode and ratio between switching and resonant frequency. When resonant converter is operating in continuous conduction mode, the beat frequency double will move according to switching frequency and eventually split when switching and resonant frequency are equal. When resonant converter is operating in discontinuous conduction mode, all poles are less frequency dependent. Position of RHP zero is limited to high frequency and doesn't need special addressing in compensation design.

Acknowledgement

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Spice Simulations of Aging Effects in Double-Gate FinFETs

Nebojša Janković, Chadwin D. Young, Miloš Marjanović

Abstract - The electrical characteristics of multi-gate field-effect transistors (FinFETs) suffer from temporal degradations due to hot-carrier injection, bias temperature instability and/or ionizing-radiation damage. The aging effects in FinFETs are mainly caused by cumulative contribution of the simultaneous generation of oxide/Si interface traps and positively charged defects within the gate oxide. The accurate capturing of the dynamic contribution of trapped charges by FinFET electrical models of circuit simulators is important for lifetime prediction and verification of long-term performance of advanced CMOS ICs. In this paper, an auxiliary sub-circuit model of the oxide and interface trapped charges will be used in Spice simualtions of the state-of-art double-gate FinFETs. The good agreement between the simualtion results and the measured change of electrical characteristics of fabricated p-type DG FinFETs under the static and dynamic NBTI tests, was obtained validating the proposed ASC model.

Keywords - Double-Gate FinFET, Trapped charge, SPICE model, device aging, circuit simulation.

I. Introduction

An excellent electrical performance of three-dimensional fin-based Field Effect Transistors (FinFETs), which includes high immunity to short channel effects and CMOS compatible processing, are the key reasons for entering this type of devices in the marketplace [1]. Apart from investigating some unique aspects of these devices, the reliability of highly scaled FinFETs for future CMOS ICs has become major concern and has continuously received the attention of research community [2,3].

Like the conventional planar FET devices, the FinFETs also suffer from temporal degradation (i.e. aging) dominated by bias temperature instability effects [4,5,6]. It arises from cumulative contribution of the generation of oxide/Si interface traps with energy density distribution D_{it} and the generation of positively charged defects in the oxide with areal density N_{ox} [6]. As an example, Fig.1 shows the experimental I_{DS}-V_{GS} characteristics of p-channel DG FinFETs extracted during the negative bias temperature instability (NBTI) stress.

The observed negative voltage shifts and sub-threshold slope degradations of I_{DS}-V_{GS} characteristics with stress time are cased by the increase of D_{it} and N_{ox} trapped charges. The appearance of the NBTI effects and device aging process implies that the accurate capturing of the dynamic contribution of D_{it} and N_{ox} by FinFET electrical models of circuit simulators is important for lifetime prediction and verification of long-term performance of advanced CMOS ICs.

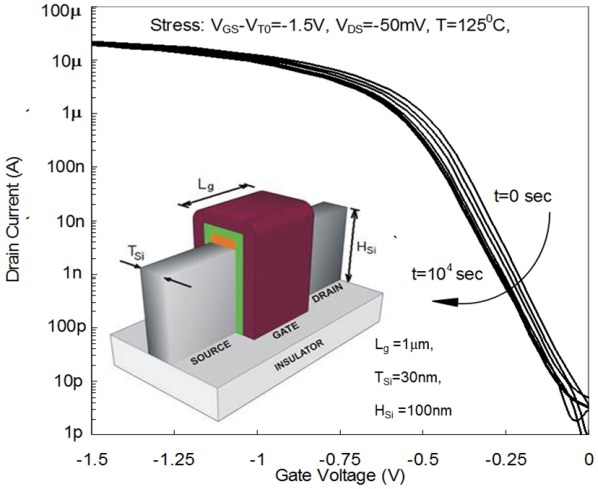

Fig. 1. I_{DS}-V_{GS} characteristics of fabricated p-channel DG FinFETs collected during the NBTI stress. The fabricated device structure is shown in the inset.

So far, the most frequently used multi-gate FinFETs electrical models implemented in Spice (*Simulation Program with Integrated Circuit Emphasis* [7]) were the first industry standard BSIM-CMG model [7,8], the University of Florida double-gate (UFDG) model [9], and the predictive technology model (PTM) [10]. All of these models, however, appear incapable to accurately predict the FinFET temporal degradation and BTI effects, since they neglect the bias-dependence of D_{it} and, moreover, omit N_{ox} as the input parameter. Recently, we have developed an auxiliary sub-circuit (ASC) aimed for proper inclusion of N_{ox} and D_{it} in Spice electrical models of double-gate (DG) FinFETs [11]. In this work, the efficiency of ASC for simulations of the NBTI effects in FinFETs will be demonstrated by comparing Spice modelling results with two dimensional numerical device simulations and the available experiments.

II. The Spice Model of Trapped Charges

In case of fully depleted DG FinFETs with two gates

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shorted (shown in the inset of Fig.1), the implicit equation was derived for calculating the channel potential ψ_s at the front and back surfaces versus the gate-source and the drain-source voltages V_{GS} and V_{DS}, respectively, as [11]:

$$\frac{1}{\gamma^2}\left[\left(V_{GS}-\phi_{ms}+\phi_{nt}-\psi_S\right)^2-\left(V_{GS}-\phi_{ms}+\phi_{nt}-\psi_S+\frac{q\cdot N_a\cdot T_{Si}^2}{\varepsilon_{Si}}\right)^2\right]=$$
$$=V_t e^{-(2\cdot\phi_b+b\cdot V_{DS})/V_t}e^{\psi_S/V_t}\left(1-e^{-\frac{q\cdot N_a\cdot t_{Si}^2}{\varepsilon_{Si}\cdot V_t}}\right)+ \qquad (1)$$
$$+V_t e^{-\psi_S/V_t}\left(1-e^{\frac{q\cdot N_a\cdot T_{Si}^2}{\varepsilon_{Si}\cdot V_t}}\right)+\frac{q\cdot N_a\cdot T_{Si}^2}{\varepsilon_{Si}}$$

where ϕ_{nt} is the flat-band correction potential. Under the assumption of uniform distribution of interface traps over the state energies within the Si bandgap, it can be expressed as [11]:

$$\phi_{nt}=\frac{q}{C_{ox}}\left[N_{ox}-D_{it}\left(\psi_s-\phi_b\right)\right] \qquad (2)$$

where also q is the elementary charge, N_a is the fin doping concentration, ε_{Si} is the silicon permittivity, T_{Si} is the fin thickness, $C_{ox}=\varepsilon_{ox}/T_{ox}$ is the gate oxide capacitance per unit area, $V_t=kT/q$ is the thermal voltage, $\phi_b=V_t ln(N_a/n_i)$ is the fin potential, $\gamma=\sqrt{(2\varepsilon_{Si}qN_a)}/C_{ox}$ is the body factor, ϕ_{ms} is the metal-to-semiconductor work function difference.

In order to obtain ψ_s versus V_{GS}, V_{DS} and N_{ox}, D_{it}, the eq. (1) has to be solved iteratively. However, the iterative method is not convenient for device compact modeling. Instead, we have recently developed an auxiliary sub-circuit (ASC) [11] that solves the eq. (1) over ψ_s using Spice simulations. Then, the new Spice model of DG FinFETs including the trapped charges is proposed [11] which combines the industry-standard Spice model BSIM-CMG [13] of multigate FinFETs and the ASC as shown in Fig.2. The ASC effectively function as an ideal voltage controlled voltage source (VCVS) producing the gate correction voltage $\Delta V_{GF}=\phi_{nt}=f(\psi_s)$ between the external and the internal gate nodes G and G*, respectively. Note that ΔV_{GF} diminishes in case of negligible trapped charges (e.g $\Delta V_{GF}\rightarrow 0$ V if N_{ox}, $D_{it}\rightarrow 0$). The ASC schematics and the derivation of model equations were discussed in details in our previous work [11].

III. Simulation Results and Discussion

In Spice simulations, the ASC block serves to correct the input voltage at the gate node of the BSIM-CMG model by the amount of $\Delta V_{GF}=\phi_{nt}$ depending on the assumed values of N_{ox} and D_{it} parameters. Fig.3 shows the comparison between measured and simulated I_{DS}-V_{GS} transfer characteristics collected at t=0 s (fresh device), 215 s and 10^4 s (the end) of the NBTI stress applied at T=125°C with V_{GS}-V_{T0}=-1.5 V, V_{ds}=-50 mV. Good matching between the model and the experiment can be observed in Fig.3 which was accomplished by tuning only the N_{ox} and D_{it} parameters of ASC. Note that a conventional NBTI "stress and sense" approach was employed as a testing method where the stress is interrupted to execute sense I_{DS}-V_{GS} measurements. The experimental p-type DG FinFET devices were fabricated on the (100) SOI substrates and with the gate wrapped around the SOI fin as shown in the inset of Fig.1. Typical device was comprised of 20 fins in parallel with gate length of 1 µm. More details of the DG FinFET design and technology can be found in [14] and [15].

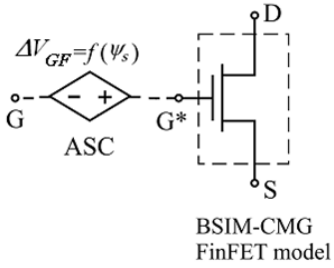

Fig. 2. Spice model of DG FinFET including the NBTI effects.

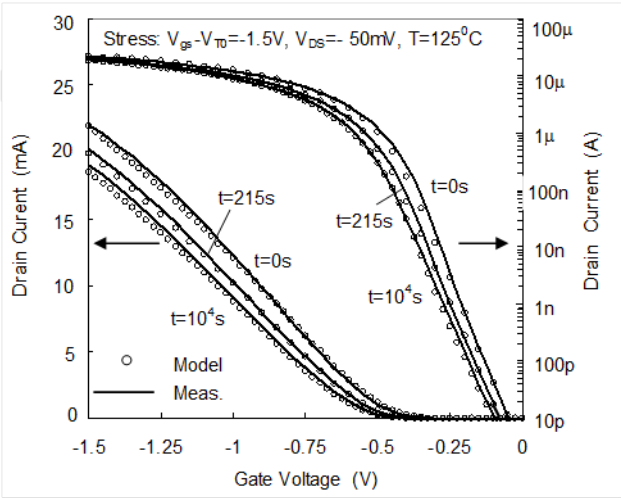

Fig. 3. Examples of measured and simulated I_{DS}-V_{GS} transfer characteristics.

Fig.4 shows the threshold voltage degradation ΔV_T versus the stress time obtained from measured and simulated transfer characteristics of fabricated p-type DG FinFET. Here, ΔV_T is defined as $\Delta V_T=V_{T0}-V_{T,\ stress}$, where V_{T0} and $V_{T,\ stress}$ holds for the threshold voltages of virgin and stressed device, respectively. The V_T extraction method was based on the maximum derivative of the g_m/I_{DS} ratio with respect to V_{GS}, e.g. $V_T=V_{GS}$ for which $d(g_m/I_{DS})/dV_{GS}=0$ [16]. This method was shown to be more

physically adequate for the advanced FinFETs with ultrathin dielectrics, double gate operation and thin SOI body, as is the case with our experimental device [16]. The ±5% error bars appearing in Fig.4 correspond to the largest relative deviation obtained between simulated and measured transfer characteristics in sub-threshold region (Fig.3).

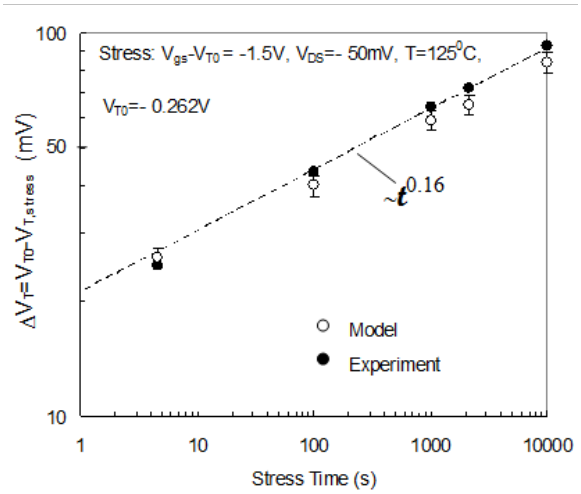

Fig. 4. The dependence of threshold voltage degradation ΔV_T versus the stress time obtained from measured and simulated transfer characteristics.

The aging effects of DG FinFETs subjected to a dynamic NBTI (DNBTI) stress can also be predicted with the ASC model providing that the time and voltage dependent functions $N_{ox}=f(V_{GS}, t)$ and $D_{it}=f(V_{GS}, t)$ are pre-determined and included in (1) and (2). The DNBTI test consists of the high-voltage pulsed periodic signal applied to a gate of FinFET at elevated temperature. During the DNBTI test, the interface defects D_{it} are generated in the on-state time period, while they partially recover in the off-state period of the pulsed signal due to traps annealing [17]. Recently, Kumar et al. [18] have proposed the analytical expressions in the form of $D_{it}= D_{it,\,0}\cdot f(t)$ that hold for time dependence of interface trap density generation in the p-type MOSFETs under the DNBTI stress. We have extended their D_{it} model to include the influence of gate voltage using the semi-empirical expression $D_{it}=A\cdot V_{st}^{m}\cdot f(t)$ where V_{st} is the DNBTI stress voltage while A and the exponent m are fitting constancies. Following the inclusion of D_{it} temporal variations in (1) and (2), we have obtained the drain current degradation $\Delta I_{ON}/I_{ON,0}$ of p-type DG FinFET with L_g=100nm and Tox=1.5nm using Spice simulations with ASC. The DNBTI test was assumed to have the pulsed gate stress signal with 50% duty cycle, 200 s time period and V_{st} of -3.4 V and -2.8 V. The obtained results are shown in Fig.5a. For comparison, Fig.5b shows the experimental results of $\Delta I_{ON}/I_{ON,0}$ obtained for conventional P-type MOSFET with identical geometry as the FinFET and with the same DNBTI test conditions as for Fig.5a. It can be observed that $\Delta I_{ON}/I_{ON,0}$ of both figures are of the same order of magnitude indicating that the aging processe of DG FinFET and planar MOSFETs under the DNBTI tests is quite similar.

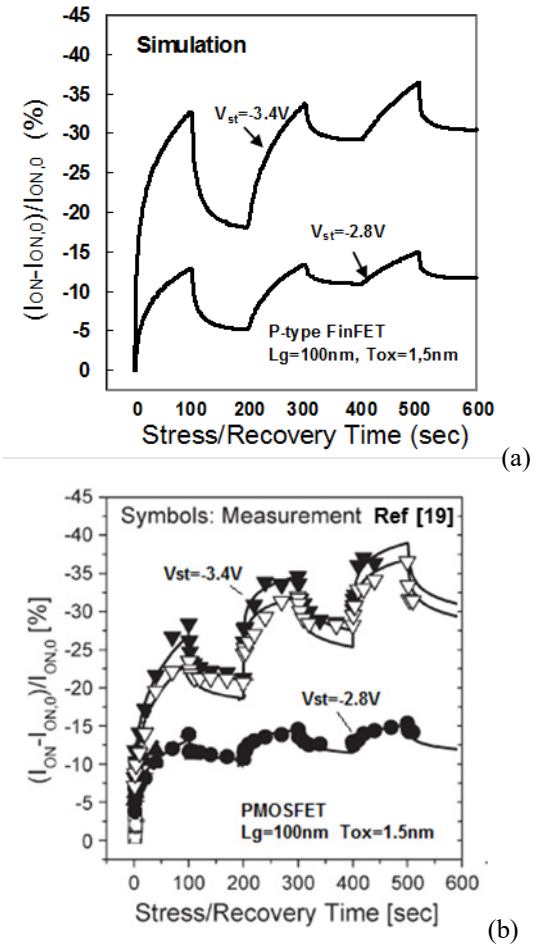

Fig. 5. Simulated (a) and measured (b) drain current degradation $\Delta I_{ON}/I_{ON,0}$ of the p-type FinFET and the planar PMOSFET, respectively, versus the DNBTI stress/recovery time, obtained for various stress amplitude V_{st}, of the 200 s period pulsed signal and with V_{ds}=-50 mV.

IV. Conclusion

A practical impelementation of the auxiliary sub-circuit (ASC) derived for Spice simualtions of NBTI effects in DG FinFETs was described in this work. The good agreement between the simualtion results obtained using the industry-standard BSIM-CMG model with ASC and the measured change of electrical characteristics of fabricated p-type DG FinFETs under the static and dynamic NBTI tests, was obtained validating the proposed ASC model.

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Modelling and simulation of standard TFRs as strain sensing elements

Ivanka Stanimirović and Zdravko Stanimirović

Abstract - In this paper modelling and simulation of standard thick-film resistors as strain sensing elements are presented. Thick-film resistors are described using a model that incorporates both deterministic model and percolation model with double percolation. The model served as a base for computer simulation of resistor behaviour under applied mechanical straining. It is shown that obtained results are in accordance with experimental ones confirming that standard thick-film resistors can be used as strain sensing elements and that presented model can be used as a tool in prediction of behaviour of mechanically strained resistors.

Keywords – Thick-film resistor (TFR), computer simulation, mechanical straining, conducting mechanisms, glass barrier width.

I. Introduction

Thick film resistors (TFRs) have been used for decades but due to their reliable performances they are still commonly used in both commercial and specialized electronics. For years they have been used in sensitive telecommunications equipment and various sensing applications. However, when micro-electro-mechanical systems (MEMS) technology emerged, thick-film technology became useful alternative for micro-machining silicon. The most MEMS are made of micro-machining silicon combining electrical and mechanical components. Such micro system might comprise one or more sensors and actuators and adequate electronic circuitry to condition the sensor signal and generate an electrical signal for actuator. Nowadays, some MEMS applications require ceramic materials in combination with thick-film technology. These MEMS are usually larger than standard and they can often be used in harsh conditions. The fact that thick-film technology can be used not only to produce the sensor and actuator elements, but to form electronic circuits for signal processing makes room for this technology in fast-growing MEMS market. When sensor applications are in question, piezoresistive effect in TFRs has been used since 1970s and over the past decade the most published papers dealt with different problems of understanding the effects of mechanical straining on TFRs [1-4] and novel thick-film compositions specifically developed for strain sensing purposes [5, 6]. However, there is a possibility that standard TFRs due to their strain sensitivity can be used in up-to-date strain-sensing applications. Standard TFRs can exhibit a rather large piezoresisitve effect that is usually undesirable property when conventional thick-film applications are in question and for this reason behaviour of thick-film under mechanical straining conditions still induces significant interest. In this paper we have performed computer simulation of changes in thick-film resistor properties caused by mechanical straining based on our previous experimental and theoretical investigations of mechanically strained standard TFRs [7] in order to predict their behaviour under applied strain.

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II. Mechanical straining of TFRs

The change of resistance in TFR under applied mechanical strain is partly due to deformation (changes in resistor dimensions), and partly due to micro structural changes resulting in specific resistivity alterations. The applied strain, ε, is defined as the relative change in the length of the resistor, while the gauge factor, GF, is defined as the ratio of the relative change in resistance and the applied strain:

$$GF = \frac{\Delta R/R}{\varepsilon} = \frac{\Delta R/R}{\Delta l/l} \tag{1}$$

The GF values for TFRs are mostly between 3 and 15. It is known that gauge factors of 2-2,5 are due to geometrical factors alone. Higher GF factors are due to micro structural changes [6]. Transport of electrical charges in TFRs takes place via complex conductive network formed during firing by sintering metal-oxide particles surrounded by glass. Our previous investigations resulted in the model of the random resistor network that was developed using the deterministic model in combination with the site percolation model with double percolation [8]. Deterministic model describes TFR as a network of conducting chains where some particles are in contact and others are separated by thin glass barriers thus forming metal-insulator-metal structures. Therefore the current flow through resistor is determined by metallic conduction through conducting particles and sintered contacts between them and tunnelling through glass barriers. Under assumption that TFR consists of M parallel conducting chains the total resistance of TFR can be given as [9]:

$$R = \frac{K_B}{M} R_B + \frac{K_C}{M} R_C \tag{2}$$

where K_B is the number of barriers and K_C the number of contacts. R_B and R_C are barrier and contact resistances, respectively:

$$R_B = \frac{h^2 s}{q^2 A (2mq\Phi_B)^{1/2}} \exp\left[\left(\frac{32\pi^2 mqs^2 \Phi_B}{h^2}\right)^{1/2}\right] \quad (3)$$

$$R_C = \frac{\rho}{\pi a} \quad (4)$$

where q and m the absolute electron charge and its effective mass respectively, h Planck's constant, s and Φ_B the potential barrier width and height respectively, $A = \pi a^2$ the barrier cross section and ρ the specific resistance of the contact. Site percolation model with double percolation introduced two percolation problems [8]:

- any lattice site can be occupied by a conducting particle with probability p or unoccupied with probability 1-p
- two neighbouring sites can be connecting by contact resistance R_C with probability p_1 or by barrier resistance R_B with probability $1-p_1$ where

$$p_1 = \frac{N_C}{N_C + N_B} \quad (5)$$

where N_C is the number of contact resistances and N_B the number of barrier resistances in TFR. Resistor, depending on its dimensions, consists of a number of elemental cells – elemental two-dimensional matrixes with N^2 elements. Within an elemental cell random occupancy of any bond between two neighbouring sites by R_B or R_C is obtained using random number generator with uniform distribution from (0,1) range – the second percolation problem. If the generated number is $\leq p_1$ then the bond is occupied by contact resistance R_C. If it is $>p_1$ the bond is occupied by barrier resistance R_B. Glass particles are being introduced using random number generator with uniform distribution to generate coordinates of glass particle centres thus removing contact and barrier resistances within the glass particle diameters D – the first percolation problem. Glass particle diameter is being obtained using random number generator with normal distribution and defined upper and lower diameter limit (3μm and 0,1μm, respectively). Diameter of the conducting particle d=150nm is being taken from the deterministic model. Such a representation of TFR incorporates both micro and macro structural characteristics of the resistor.

III. Simulation Results and Discussion

Simulation of standard TFRs as strain sensing elements was performed using model described in section II in combination with experimental results obtained during series of experimental investigations related to behavioral analysis of thick-film resistors subjected to mechanical and electrical straining. Detailed description of performed experiments can be found in [7]. These investigations confirmed assumption that the tunneling process through glass barriers gets higher strain sensitivity than metallic conduction. This means that this type of straining can only influence the barrier resistance changing the glass barrier width since numbers of contacts, barriers and barrier height cannot be influenced by this type of straining. For simulation purposes we chose to evaluate 1mm wide and 2, 4 and 6mm long resistors centrally positioned on the substrate with fixed edges (Fig. 1) subjected to maximal mechanical straining of 400μm resulting in changes of resistor physical dimensions shown in Table I.

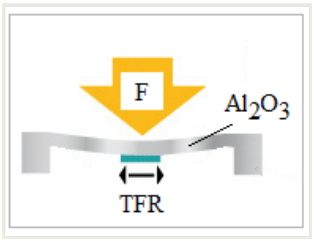

Fig. 1. Schematic presentation of experimental settings

Sheet resistances of 10kΩ/sq and 100kΩ/sq (Fig. 2) were selected with 0,2 and 0,1 volume fractions of conductive phase respectively. Resistor composition with sheet resistance of 1kΩ/sq was excluded because of the small conducting/isolating phase ratio that determines dominant conducting mechanism – conduction through clusters of particles that cannot be affected by mechanical straining [7].

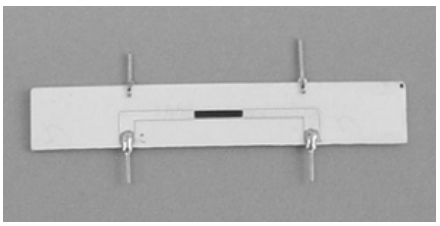

Fig 2. One of TFRs used in the experiment (w=1mm, l=6mm, R_{sq}=100kΩ/sq)

Potential barrier height Φ_B=1V and initial value of barrier width s=1,33nm were taken into account. These values were used, along with experimentally obtained resistance values for unstrained TFRs [7], to simulate resistor microstructure – number and spatial distribution of contact and barrier resistances. Then, microstructure of strained resistor was being simulated based on experimentally obtained percentual changes in resistance values after performed mechanical straining. Having in mind that mechanical straining affects the charge transport by changing glass barrier widths, as an illustration of performed simulations relative changes of barrier widths due to mechanical straining are presented in Fig. 3 and 4.

TABLE I
EXPERIMENTAL VALUES USED IN SIMULATIONS [7]

R_{sq} (kΩ/sq)	10	10	10	100	100	100
R_i (kΩ)	16,59	32,81	50,64	276,51	495,83	704,3
l (mm)	2	4	6	2	4	6
$\lvert \Delta R \rvert$ (%)	0,958	0,945	0,918	1,381	1,266	1,136
Δl (μm)	1,905	3,81	5,175	1,905	3,81	5,715

In Fig. 3 relative changes of barrier widths vs. relative changes of resistor lengths for mechanically strained TFRs of the identical initial length and different sheet resistances are given. It is shown that higher sheet resistance suffers grater barrier width change due to lower conductive/glass phase ratio and therefore more dominant tunnelling mechanism. Also, barrier width increases with the increase in length of the strained resistor (Fig. 3).

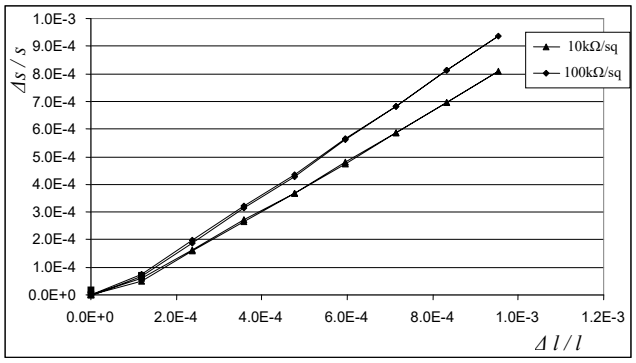

Fig. 3. Relative change of barrier widths vs. relative change of resistor lengths for 4mm long mechanically strained TFRs with nominal sheet resistances of 10kΩ/sq and 100kΩ/sq and initial value of barrier width s=1,33nm

Relative changes of barrier widths for TFRs with different initial lengths and sheet resistances are given in Fig. 4. It can be seen that that shorter resistors exhibit greater barrier width changes. In order to prove that these results are in accordance with experimental results GF values were calculated (Fig. 5). Experimental results show that resistor compositions with smaller volume fractions of conducting phase have greater GF values. TFRs based on 100kΩ/sq composition have lower volume fraction of conductive phase than 10kΩ/sq composition and therefore its charge transport is predominantly limited by conduction through glass barriers. TFRs based on 10kΩ/sq composition incorporate approximately equally tunneling through glass barriers and conducting through conducting particles and sintered contacts. Fig. 5 shows that obtained GF values are greater for resistors realized using compositions with higher sheet resistance but decrease with increase in length for resistors with identical nominal sheet resistance. It can be noticed that TFRs realized using 10kΩ/sq composition have GF~10 and therefore can be used as strain sensing elements.

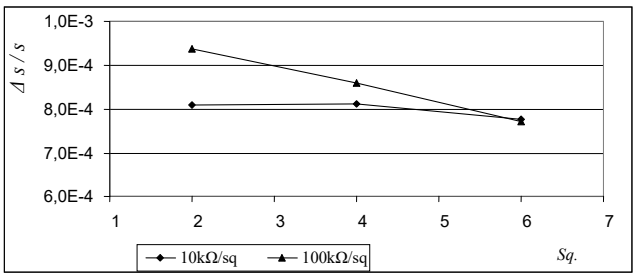

Fig. 4. Relative change of barrier widths vs. resistor area for mechanically strained TFRs with different initial lengths and nominal sheet resistances of 10kΩ/sq and 100kΩ/sq

Simulation results proved to be in accordance with experimental results proving that applied model can provide adequate analysis of mechanically strained TFRs. Depending on the application, data basis could be formed that would incorporate all necessary data about the resistor composition to be used, straining conditions that are to be applied and expected percentual resistance change for every composition. In that way behavior of strained TFRs can be predicted and used during the design phase of the device or in reliability assessment. Another potential use of this simulation process is analysis of degradation processes and failure mechanisms in TFRs subjected to various types of straining. It may be possible to introduce presence of defects in the model of TFR structure thus predicting its behavior under various straining conditions both mechanical and electrical. Such an analysis could be of use in performance optimization and elimination of potential reliability issues.

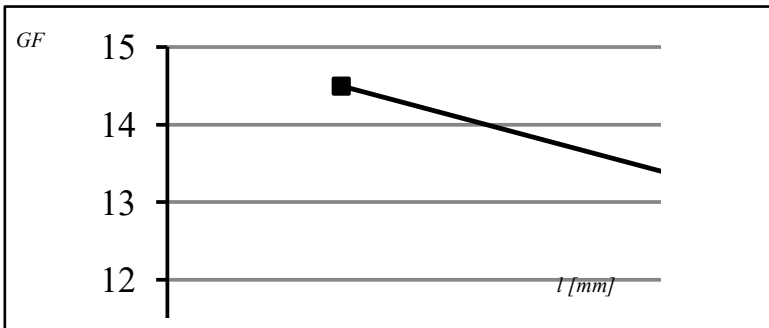

Fig. 5. Mean values of gage factors for TFRs with different lengths and sheet resistances of 10kΩ/sq and 100kΩ/sq

IV. CONCLUSION

In this paper modelling and simulation of standard TFRs as strain sensing elements are presented. A model that incorporates both deterministic model and model based

on percolation theory is being used in order to represent spatial distribution of conducting and isolation phase within the volume of these complex heterogeneous structures that determines types of conducting mechanisms and basic characteristics of resistive layers. Deterministic model introduced micro structural and percolation theory introduced macro structural characteristics of the resistor into the model. In order to investigate whether standard TFRs can be used as strain sensing elements described model was used for computer simulation of thick film resistors subjected to mechanical straining. Resistors with sheet resistances of 10kΩ/sq and 100kΩ/sq, previously used for experimental investigations [7], were simulated. Obtained results were compared with the results of experimental analysis and it is proved that mechanical straining causes reversible resistance change due to change in conduction conditions. It causes the barrier width change thus affecting conducting through glass barriers. It is shown that standard resistors can be used as strain sensing elements, particularly TFRs based on 10kΩ/sq composition and that presented model can be used in prediction of behavior of mechanically strained TFRs. That can be of use in various stages of device design as well as in reliability analysis. Because the applied model incorporates both micro and macro structural characteristic of TFRs, further investigations may be directed to simulation of degradation processes in resistors caused by different types of unwanted straining in order to study these processes.

ACKNOWLEDGEMENT

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ANN Model of High Electric Field Stress in n-channel VDMOS Power Transistors

Aleksandar Vulović, Milan Savić, Sanja Aleksić, and Dragan Pantić

Abstract - One of the most common causes of unstable operation of power VDMOS transistor is the exposing of the gate oxide to high electric field, which happens when the voltages, whose the values are similar to the breakdown voltage, are conducted onto the gate contact. Processes that are occurring in the oxide and semiconductor bulk and at the Si/SiO_2 interface are very complex and it is therefore impossible to create an acceptable and accurate physical model to describe the device characteristics. In this paper, we have applied artificial neural networks (ANN) for modeling and simulation of high electric field stress (HEFS) in n-channel VDMOS power transistor. To build ANN HEFS-nVDMOS model we used measured transfer characteristics $I_D=f(V_{GS})$, for different times of stress. Different neural network structures were tested and optimized to obtain the best ANN HEFS-nVDMOS model configuration[1].

Keywords – neural network, n-channel VDMOS, simulation, model, high electric field stress.

I. Introduction

There are problems in electronics that are very complex so it is almost impossible to define the corresponding unique physical model to describe these phenomena. That is why we will have to neglect some effects in the process of generating models, and therefore we have taken into account when to apply the appropriate model. On the other hand, even if we could generate a physical model of satisfactory accuracy, it would be so complex and practically inapplicable in TCAD software tools for process, device and circuit simulation. Effective solution, which imposes in cases like this, is the application of models which are generated by using the artificial neural networks (ANN). In contrast to traditional models, which are *theory-rich* and *data-poor*, ANN models are generated in a way that a little or no a priori knowledge of the problem is required [1-3].

ANN model design process consists of seven basic steps (Fig. 1) [4]. The first step is data collection. This procedure is realized independently of software tools which are used to generate the ANN model, but this step is critical to the success of the design process. Therefore, it is very important to carefully design and realize the experiment that will provide us with the necessary number of required data. After a neural network has been created, which means to arrange the network to be compatible with our problem that we want to solve (step 2), it needs to be configured (step 3). After that the adjustable parameters of neural network (weights and biases) are first initialized (step 4) and their values are optimized and carefully tuned. This process is called neural network setup or training (step 5). Finally, we have the process of validation of the generated ANN model (step 6) and its use (step 7), if all tests have been successfully verified.

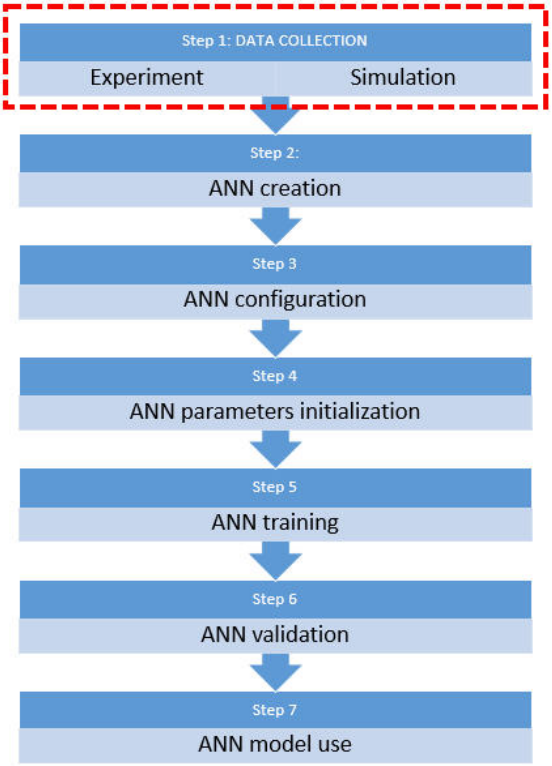

Fig. 1. The work flow for ANN model design [4].

When the high voltage, close to the breakdown voltage, acts on the gate contact, the instability of the VDMOSFET electrical characteristics occurs [5-9]. The charges which are generated in the gate oxide and at the Si/SiO_2 interface dominantly influence on the threshold voltage of VDMOS transistor. Processes that are occurring in the oxide and semiconductor bulk and at the Si/SiO_2 interface are very complex and it is therefore impossible to create an acceptable and accurate physical model to describe the device characteristics. In this paper, we will apply ANN for modeling of high electric field stress (HEFS) in n-channel

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VDMOS power transistor. To build ANN HEFS-nVDMOS model we will use measured transfer characteristics $I_D=f(V_{GS})$, for different times of stress in the range from 0 to 150 minutes. Different neural network structures will be test and optimize in order to obtain the best ANN HEFS-nVDMOS model configuration.

II. Neural Network Model Design

A. Data collection

Once a research problem has been determined the next step is to identify which method will be appropriate and effective for data collection. In our case there are two sources of data necessary for ANN model design. Primary data collection uses experimental results. The commercial n-channel VDMOS power transistor IRF510 [10] has been exposed to HEFS by V_S=80V on the gate contact for up to t_S=150 minutes (Fig.2). The transfer characteristics $I_D=f(V_{GS})$ is measured at defined time intervals at room temperature (T=25°C).

The secondary data source can be the results obtained by simulating the electrical characteristics of n-channel VDMOS power transistor under the influence of HEFS.

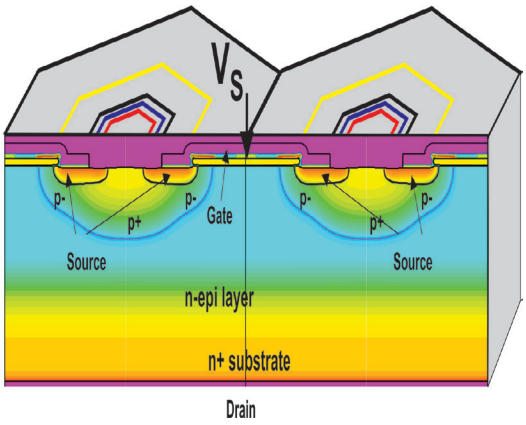

Fig. 2. The cross section of n-channel VDMOS power transistor.

B. ANN creation and configuration

ANN model creation assumes that neural network corresponds to the problem we want to solve. In this case, we want to form a model that will be able to give us the transfer characteristics $I_D=f(V_{GS})$ of n-channel VDMOS power transistor IRF510 which is exposed to HEFS. According to that, the input parameters of ANN HEFS-nVDMOS model are: stress voltage V_S, time of stress t_S and gate voltage V_{GS}, while the output parameter is drain current I_D. The block diagram of the proposed ANN HEFS-nVDMOS model is given in Fig. 3. Hence, our ANN model has 3 neurons in input layer (IL) and 1 neuron in output layer (OL). The structure and number of neurons in hidden layers (H1, H2) will be optimized in order to obtain the best ANN model accuracy.

Within the neural network configuration the definition of the connections between components of the network is required. In our model there is a bias connected to each layer, inputs are connected to H1 and output comes from H2. Layers H1 and H2 are also connected. After a neural network has been created, it must be configured. It is necessary to define example data set of inputs and targets (desired ANN model outputs). It is very important to know that ANN model can only be as accurate as the data that are used to train the neural network. The defined sample data must first be processed. We need the minimum and maximum values of the defined data to perform the correct normalization so that all inputs fall in the range [-1,1] or [0,1].

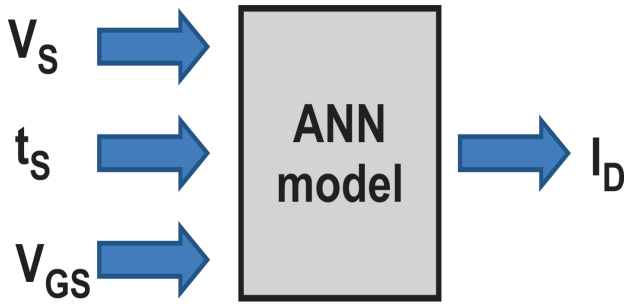

Fig. 3. The proposed ANN HEFS-nVDMOS model.

C. ANN training and validation

ANN training can be more efficient if preprocessing steps on the sample data are performed. Typically, the normalization is applied to both the input and target data set. In that case, when ANN model is put to use output results fall into a normalized range and it is necessary to transformed it back into the units of the original target data. It is important that the data cover the range of inputs for which ANN model will be used. The data are first divide into three subsets: training set, validation set and test set. Training set is used for computing, tuning and updating the network weights and biases. Finally, after the initialization of the network weights and biases the ANN is ready for training.

The training process of ANN implies tuning the values of the weights and biases in order to optimize neural network performance and minimize sum square error (SSE). SSE is defined as sum squared error between ANN model outputs and target outputs. In our model we use Levenberg-Marquardt and Bayesian training algorithm. In hidden layers tan-sigmoid transfer function is used, while neurons in output layer have linear transfer function. ANN HEFS-nVDMOS model is tested with one and two hidden layers, while the number of neurons in these layers is changed from four to nine. Sum squared errors for different ANN model structures for train and test data sets are given in Table I. It is obvious that the best result is obtained for the network with two hidden layers with seven and nine neurons in H1 and H2, respectively. Schematic diagram of HEFS-nVDMOS neural network is shown in Fig. 4.

TABLE I
SUM SQUARED ERROR (SSE) COMPARISON FOR DIFFERENT ANN STRUCTURE

ANN structure				SSE	
IL	H1	H2	OL	**TRAIN**	**TEST**
3	4	0	1	0.089931285	0.068499754
3	5	0	1	2.954554294	2.647080672
3	6	0	1	0.112300972	0.093437814
3	7	0	1	0.014032776	0.061402315
3	8	0	1	0.017724825	0.047014735
3	5	5	1	0.006783653	0.010740525
3	6	6	1	0.001738477	0.002346667
3	7	7	1	0.001709225	0.009891808
3	7	8	1	0.000926591	0.605611541
3	7	9	1	0.000325886	0.001180359
3	8	8	1	0.000230926	0.004370062

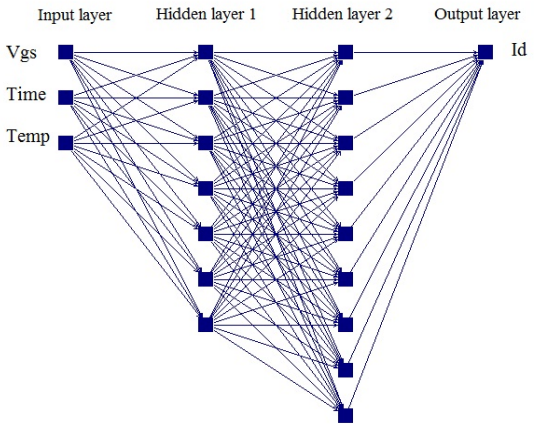

Fig. 4. Schematic diagram of HEFS-nVDMOS neural network.

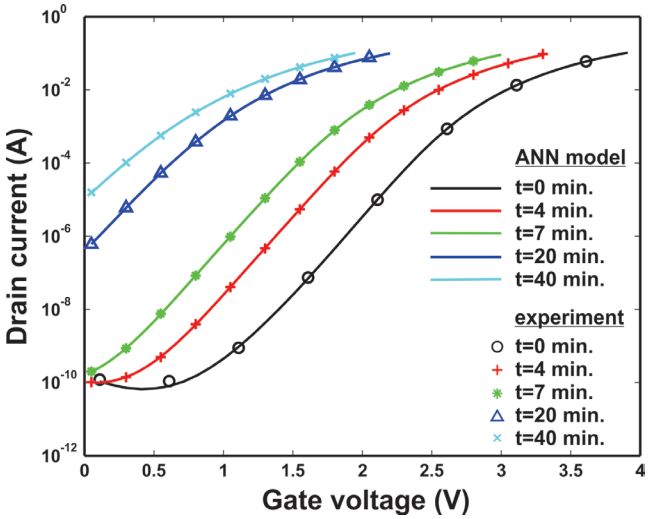

Fig. 5. Transfer characteristics $I_D=f(V_{GS})$ of n-channel VDMOS power transistor IRF510 under HEFS with V_S=80V: ANN model (solid lines) and experiment (marks).

III. RESULTS AND DISCUSSION

When the training of neural network is complete it is necessary to check its performance and determine if any changes need to be made. After the network is trained and validated, ANN model can be used to calculate the response to any input. In our case ANN HEFS-nVDMOS model gives the transfer characteristics $I_D=f(V_{GS})$ of n-channel VDMOS power transistor IRF510 after the influence of V_S=80V on gate contact for an arbitraty time of stress t_S up to 150 minutes.

The comparison of transfer characteristics obtained with ANN HEFS-nVDMOS model with experimental results which were used for neural network training are shown in Fig. 5 and Fig. 6. A very good agreement is obtained, which is expected, considering the value of SSE which is given in Table I.

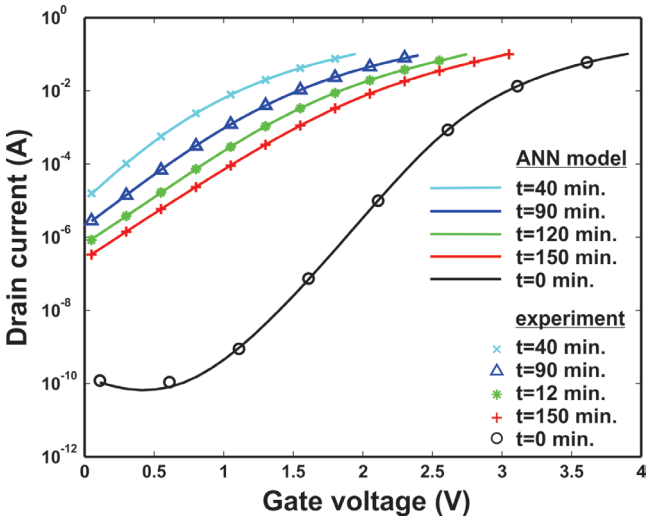

Fig. 6. Transfer characteristics $I_D=f(V_{GS})$ of n-channel VDMOS power transistor IRF510 under HEFS with V_S=80V: ANN model (solid lines) and experiment (marks).

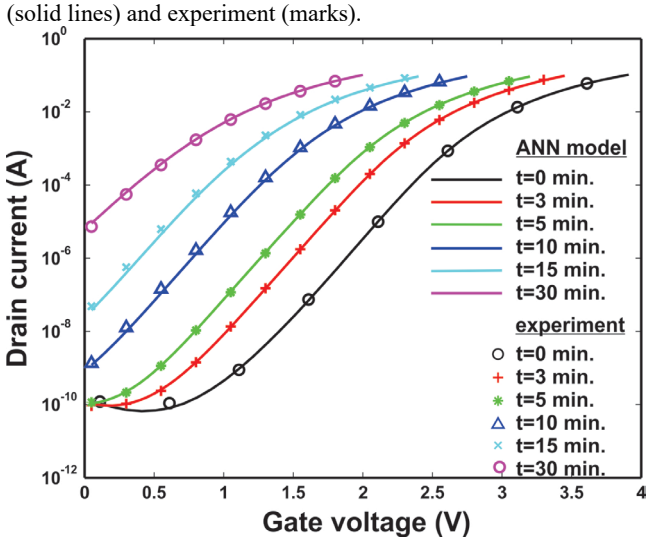

Fig. 7. Transfer characteristics $I_D=f(V_{GS})$ of n-channel VDMOS power transistor IRF510 under HEFS with V_S=80V: ANN model (solid lines) and experiment (marks).

In Fig. 7 and Fig. 8 we made a comparison of transfer characteristics obtained with ANN model with the experimental results that have not been used in the process of neural network training. As in the previous case, very good agreement is obtained, which indicates hat the neural network is well trained and that the generated ANN model can generalize well within the range inputs for which the network has been trained.

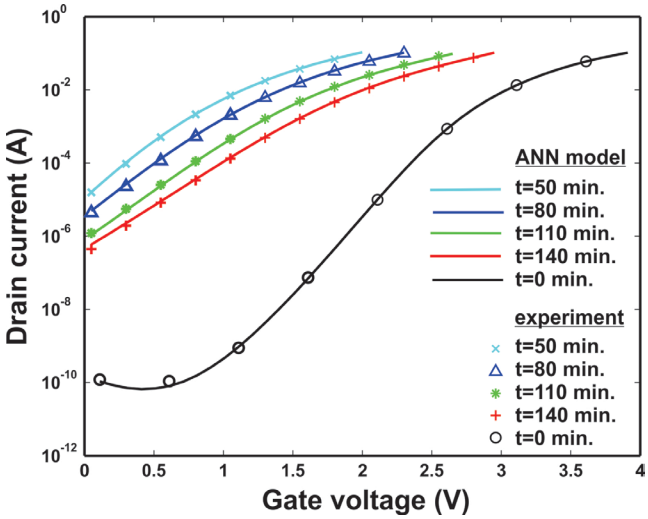

Fig. 8. Transfer characteristics $I_D=f(V_{GS})$ of n-channel VDMOS power transistor IRF510 under HEFS with V_S=80V: ANN model (solid lines) and experiment (marks).

V. Conclusion

In this paper, we have applied ANN for modeling of high electric field stress (HEFS) in n-channel VDMOS power transistor. To build ANN HEFS-nVDMOS model we used measured transfer characteristics $I_D=f(V_{GS})$, for different times of stress (t_S=0 to 150 minutes). Different neural network structures were tested and optimized to obtain the best ANN model configuration (IL=3, H1=7, H2=9, OL=1) with a minimum SSE. The proposed ANN model gives very good agreement with the experimental results. This indicates on the great possibilities of the application of the models based on neural networks in this area.

Acknowledgement

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ANN solution for increasing the efficiency of tracking PV systems

Duško Lukač and Miljana Milić

Abstract - The purpose of the this research is to build up a system model using artificial neural network (ANN), which should be used to forecast the performance of a tracking solar cell in compare with a fixed positioned cell, by taking into account the outside temperature and light radiation. In this way, one can perform an annual profit comparison as well as the prediction in order to decide whether a tracking PV cell is worthwhile or not. The network was trained using the Cologne weather data collected during one day measurements on a particular Polycristal solar module. The first obtained results have shown that this idea can be considered promising and should be further exploited.

Keywords - Policrystal PV cell, Feed-forward artificial neural networks, Solar cell tracking system.

I. Introduction

The efficiency is one of the most problematic issues in solar cell manufacturing and exploitation. During last few decades, many attempts were made in different scientific disciplines to improve it. Bell Laboratory fabricated the first crystalline silicon solar cells in 1953, achieving the efficiency of 4.5% [1], [2], [3]. Those early PV cell fabrication technologies suffered from high cost, low stability, manufacturability, durability and/or toxicity [4]. Due to constant research effort in this area, these values were changing slowly but unquestionably during many years.

Depending on the production technology, solar cells can be divided into two groups: ones produced from Si wafers i.e., silicon solar cells and others, produced with vacuum technologies i.e., thin-film solar cells. According to the crystalline structure, amorphous, poly-crystalline and mono-crystalline solar cells can be distinguished. In order to build solar modules with power range of two hundred watts or more, solar cells are being connected together. For large PV systems special PV modules are produced with typical power range of up to several hundred watts. The solar module properties depend mainly on the type of the applied solar cell [5].

The improvements in fabrication technology and materials are welcome and expected, since large amounts of money goes for this research. But our aim here is to show that good efficiency improvements can be achieved at the application side of PV modules as well.

Basically one can increase the yield of a solar cell device by actively turning the solar generator to the sun. However, the tracking system increases only the direct radiation component, while the diffuse radiation remains nearly unchanged. As an example Fig. 1 shows the day yields of a tracked solar cell and a fixed one during two different days. During the sunny day the tracked solar cell can increase the energy profit for nearly 60%. Nevertheless, in the case of a cloudy day the yield of the tracked arrangement is approximately 10% less then with the fixed system arrangement. The reason for this lies in the fact that the tracked modules can stand at an acute angle in the morning and in the afternoon and therefore receive vague radiation.

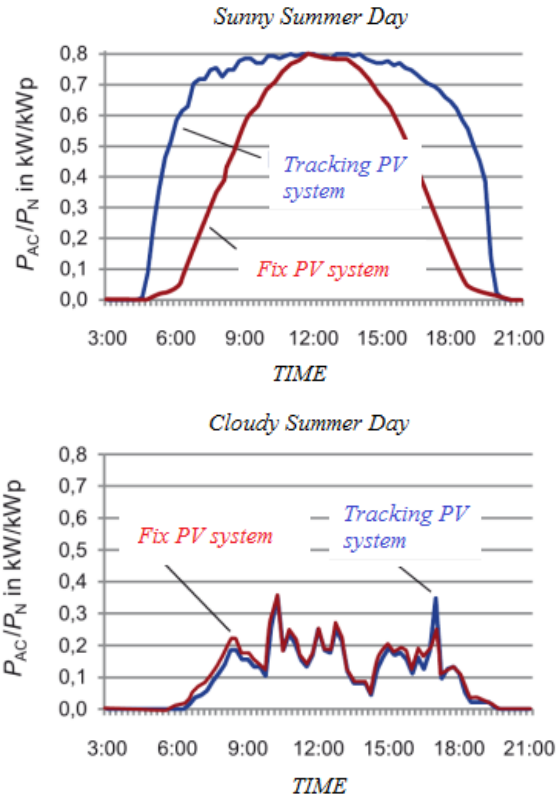

Fig. 1. Yield comparison between fixed and tracked PV cell by different weather conditions

More than half of the annual global radiation in Germany can be categorized as the vague. That's why the

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profit win of tracking solar cell systems is limited to approximately 30%. Hence, the application of tracking solar cell systems should be considered with respect to additional mechanical and electric expenditures. One example of the tracking PV system is shown in Fig. 2.

Fig. 2. 2-axis PV tracking system (Mover M100)
Source: http://www.pv-mover.com/tl_files/pv_mover/images/PVMover%202010/ MG_9663kl.jpg

To realize a comparison of yields with and without construction of the tracking solar arrangement, an artificial neural network will be trained. The network should perform the prediction of the profit win when tracked solar arrangements are observed, in order to decide, whether they should be used or not.

II. Preparation of Input Data and Calculation of Outputs

The feed-forward ANN model, which is to be developed using the principles of the supervised learning, needs a large number of input-output data pairs in order to represent the required function. The number of all possible input-output data pairs can be calculable, since the large amount of data for ANN training would last unacceptably long, regardless of the used arithmetic system. For modelling of the artificial network, the sufficient number of training pairs can be calculated according to various criteria. For example, the number of training pairs (TP) as reported by [6], depends on the number of neurons in input, hidden and output layer of the ANN. On the other hand, the number of TP, according to [7] depends on the number of weights (W) and acceptable testing errors (ε) and is calculated as: $N > \frac{W}{\varepsilon}$. This rule is not used in our study because of the lack of necessary data. In order to obtain required value for TP, the number of the hidden neurons must be considered. For the calculation of the number of hidden neurons different criteria can be tested, such as those described in [8] and [9]. Because of relatively small number of input and output neurons for our purpose, criteria by [9] appear to be more fitting. The number of hidden neurons taking into account 4 input and 3 output neurons, according to chosen criterion is therefore shown in the following table:

TABLE I
Calculation of the Number of the Hidden Neurons and Training Pairs

Reference	Number of hidden neurons	Minimal number of training pairs (TP), by [6]
[9]	H = 1 ... 3 * 4 = 4 ... 12	TP = 5 * ((4*4)+(4*3)) = 140 → minimal case 900 → maximal case

The number of TP, which is calculated as described in [6], is also shown in the table. As stated in [6] there should be at least 5-times more training pairs than weights. Therefore the following minimal and maximal TP values arise:

- Minimal = 140
- Maximal = 900

With the calculation of training pairs, confirming to chosen expert's criteria, we plan to reach at least the minimal number of TP, while in the optimal case, the maximal number of TP. With total amount of 658 available training pairs in this work, it can be assumed that we are in the good middle. The preparation of the input values is carried out with the help of the Excel programme.

III. Data Normalisation

Dependent and independent variables, as well as the criteria of their goodness, are defined with respect to values that may differ numerically and in meaning. If these values were fed into an ANN without normalisation, the net would be wrongly trained considering its weights because such weights could not represent the input and output (result) relations, neither numerically nor by the meaning. The weight's change depends on the "height" of the derivation of the neuron activation function and for the case of very small and very large input values of logistic function behaves in the same way, i.e., is constantly equal to zero. Consequently, no weight change arises during the training process, which leads to failure in learning. Therefore, ranges of input values should be made narrower, while the appropriate input connection weights should also be kept small. Hence, the input beside small initial weights and learning rates should also have small span. Such a phenomenon is called "Saturation" of the ANN [10].

In order to achieve equal level of weights accommodation for different ANN layers, a pre-processing of all used values of the input vector is necessary. This process is called normalisation or standardisation, and it guarantees the comparability of the data. There are many different suggestions for the standardisation of the input or output values. Some of the standardisation methods are described in [11], [12] where normalisation procedure can be calculated as (1):

TABLE II
SYSTEMATIZATION OF THE ANN TRAINING DATA

Input1	Input2	Input3	Input4	Output	Output1>10%	Output2>30%	Output3>50%
I [mA]	U [V]	Outside temperature	Weather/ Light	Pn [W]/ P [W]	Efficiency increase with a tracked module > 5%	Efficiency increase with a tracked module > 10%	Efficiency increase with a tracked module > 20%
fixed (normalized)	fixed (normalized)	°C (normalized)	sunny (0,9); cloudy (0,5), raign/dark (0.1) (normalized)	tracked in % (normalized)			
0.389473684	0.9375	0.48	0.5	0.07998908	0.07998908	0	0
0.392982456	0.943181818	0.48	0.5	0.063898451	0.063898451	0	0

$$SV_{VV} - TF_{min} + \left(TF_{max} - TF_{min}\right) \cdot \frac{D - D_{min}}{D_{max} - D_{min}} \cdot V \quad (1)$$

Description of the abbreviations:

- SV - Scaled Value
- TF_{min} and TF_{max} - minimal and maximal value of the transfer function
- D - observed values
- D_{min} and D_{max} = minimal and maximal values of the observation

The highest value can therefore be at least 1, and the lowest value 0. Besides, the absolute value is the one to be followed. The addition of the negative TF_{min} value occurs in the form of the reverse array of the values. Therefore the values of input and output vectors are normalised taking into account the use of the logistic function. The normalisation of input or output values can be carried out by applying the framework used at Rheinische Fachhochschule-Koeln, for example. In this research, training pairs are standardised before the net training.

IV. DESIGN OF THE ANN, TARGET NET ERROR AND RESULTS

Designed ANN is presented in Fig. 3. The selected topology represents a feed-forward ANN cell with one hidden layer, containing four input, eight hidden and tree output neurons.

A small part of training data obtained after normalization can be systematized in the Table 2.

Before the net training, the TPs have been separated into the training, test and validation set according to ration 70:20:10. The net learning has been carried out conforming to Resilient Backpropagation (RPROP) algorithm defined in [13]. Target net error for "auto teacher" has been set to 2%. Training has been performed with Intel Pentium 2020M, 2.4 GHz processor PC, and took 45min till the target values have been reached. The target net error graph is shown in Fig. 4. The target net error is satisfied after the training.

When the ANN training is complete, it has been tested with the test set and validated with the validation set. Definition of the test set is presented in Fig. 5.

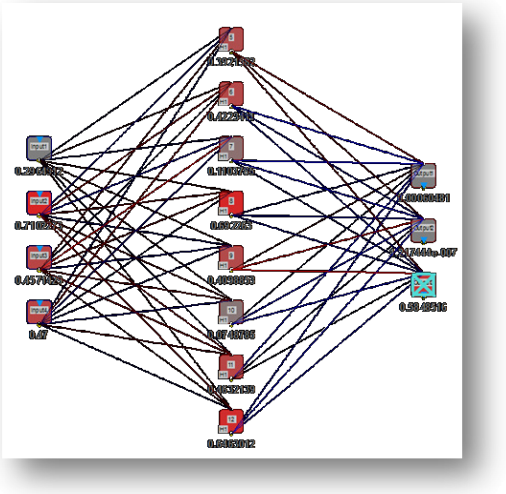

Fig. 3. Architecture of the used ANN

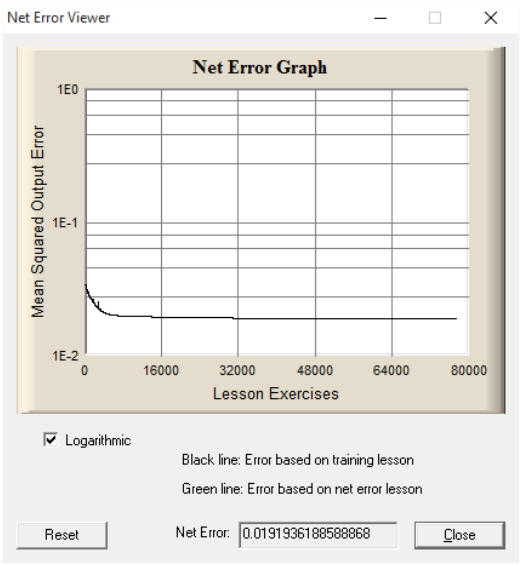

Fig. 4. Target net error graph

In the particular case of the input values, the Output 3 has to be activated (increase of the performance > 20%).

This situation is shown in the Fig. 6.

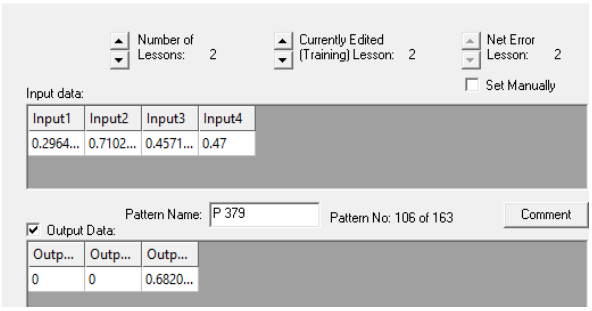

Fig. 5. Definition of the test set

In Figs. 7, 8, and 9, the target and current output activation of the output neurons 1, 2 and 3, respectively are presented. By observing the following figures, it can be concluded that the training of the output neuron 2 is optimal, while trainings of output neurons 1 and 3 are very good, but may sporadically have some values which can be optimised. This can be done, by optimising the architecture of the ANN or/and using additional representative TPs.

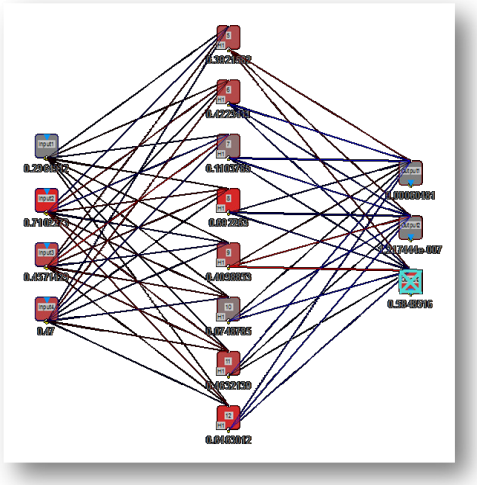

Fig. 6. Test results and expected activation of Output 3

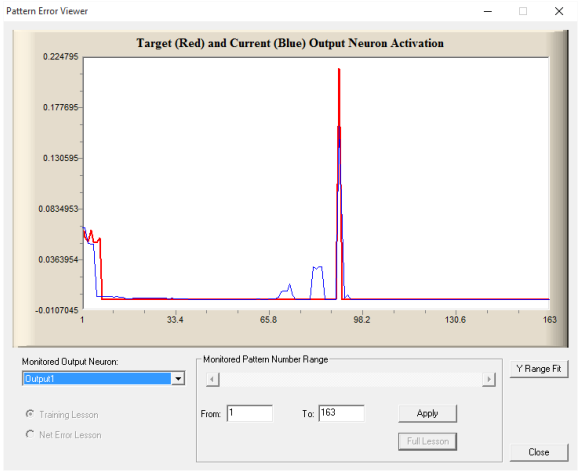

Fig. 7. Pattern error graph of the Output neuron 1

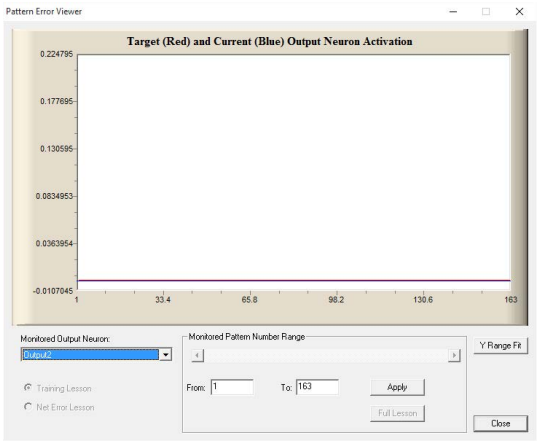

Fig. 8. Pattern error graph of the Output neuron 2

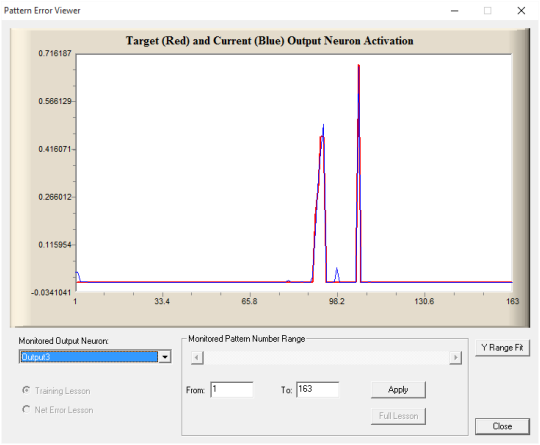

Fig. 9. Pattern error graph of the Output neuron 3

Limitations of the work

Main limitation of the work is the lack of data, since the net was trained by taking into consideration data which represent only partially annual behaviour and whether data for the Cologne area. In order to build up usable ANN, the annual data should be used for the net training.

V. Conclusion

Regardless of the limitations of this research, the architecture, the way how to train it, and training results of the ANN used for the comparison of the yield increases with and without construction of the tracking solar arrangement, have been presented in this paper. Further work will be oriented to net optimization by using the representable annual set of training pairs.

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Model of High Efficiency Solar System with DC/DC converter

Branko Blanuša, Željko Ivanović and Branko Dokić

Abstract - Model of high efficiency solar system with photovoltaic (PV) panel, DC/DC converter and 24V DC load is presented in this paper. Control modul is realized with fuzzy controller. This controller controls duty factor and switching frequency of the converter. In this way the solar system works with applied maximum power point tracking (MPPT) algorithm and switching frequency which provides converter work with maximum efficiency. Functionality of proposed model is confirmed through computer simulations in Matlab.

Keywords - Model, Solar system, fuzzy controller, MPPT, efficiency optimization.

I. Introduction

Electrical energy production from renewable energy sources, increasingly grows and significant, one can say the leading, place have solar panels. This method of power generation from solar systems is one of the cleanest and safest, and there is no acoustic pollution that is characteristic for wind plants.

Although new materials and production techniques of photovoltaic cells were developed, silicon is still in over of 80% the produced photovoltaic cells. The reason is wide accessibility of silicon and the fact that it is not toxic. Monocrystalline and polycrystalline photovoltaic (PV) cells are two basic types of silicon photovoltaic cells. There is a third type, amorphous silicon, but the efficiency of these cells is lower than in the previous two types and is less used. Most photovoltaic cells are monocrystalline type. The efficiency of these solar cells is 15-20%. Efficiency of polycrystalline cells is lower and around 12-15%. Production process of photovoltaic cells of amorphous silicon is simpler than the previous two. However, the drawback is the poor efficiency, which ranges from 6-8% [1].

One of the basic requirement that is set in front of solar systems is their efficiency. Therefore, there is an intensive research that is carried out into several directions:

- Development of materials for solar panels with a better ratio efficiency/price.
- Optimization of solar system topology from the standpoint of electrical energy production and consumption.
- Maximum utilization of available power of solar panels.
- Maximum efficiency of power converters used in solar systems.

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Application of DC/DC converters in solar systems are wide and significant. Over these converters solar panels are connected to DC consumers. Also these converters can be used as battery chargers, or interfaces between solar panels and DC/AC converters. The proposed algorithm is applied to a simple solar system consisting of solar panel, boost DC/DC converter and 24V DC consumers (Fig1.), although it can be used in more complex solar systems and for different types of DC/ DC converters.

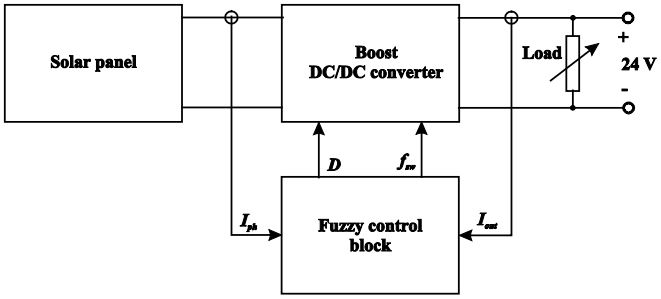

Fig. 1. Block diagram of the realized solar system

Central place in this paper has control module with fuzzy controller. It controls the DC/DC converter so the MPPT algorithm is applied. Also, for a given operating conditions swiching frequency is adjusted, so the converter operates with maximum efficiency.

Organization of paper is as follows: Loss model of boost DC/DC converter, and its dependence from the switching frequency is described in the second chapter. The realization of the fuzzy controller for implementation of MPPT algorithm and converter efficiency optimization in a solar system is presented in the fourth chapter. Work of the proposed controller is tested through computer simulation. The results are presented in the fifth chapter. Obtain results are summarized in conclusions.

II. Boost Converter Losses

Boost DC/DC converter is realized in this solar system where standard topology of this converter is often used [2] (Fig1.).

Energy losses in elements of the boost converter can be divided into: conduction, dynamic and fixed losses. Total energy loss P_{loss} is expressed as [3]:

$$P_{loss} = P_{cond} + P_{fixed} + W_{TOT} \cdot f_{sw} \quad (1)$$

where: P_{cond} – conduction losses, P_{fixed} – fixed losses, W_{TOT} – total energy of dynamic loss during one switching period. Product $P_{sw} = W_{TOT} \cdot f_{sw}$ is average value of dynamic power loss, which is directly proportional to switching frequency f_{sw}. Conduction losses are directly dependant on loads, and very little dependant on switching frequency. Fixed losses are dependent on neither switching frequency nor load. They are consisted of controller power supply current, and leakage currents of transistor, diode and capacitors. These losses are often much less in comparison to conduction and dynamic losses, so these can be neglected.

Semiconductor elements are major source of dynamic losses in the converter. During switching transitions, very high power losses can occur in semiconductor devices. Although the switching time of semiconductor elements is very short, average power loss can be substantial. Dynamic losses are very little dependent on power load, but directly depend on switching frequency.

Equivalent scheme of boost converter is presented on Fig. 2. MOSFET is used as basic switch component. It is assumed that the converter elements are linear, and time, frequency and temperature independent.

Turned on MOSFET is modeled with R_{ON}, while diode is modeled with serial connection of voltage source V_D and resistance R_D. Input MOSFET capacitance C_{iss} and output capacitance C_{oss} are also included in the model. The input generator is modeled with serial connection of internal resistance R_{GEN} and the ideal voltage generator. Equivalent losses in converter supply circuit are presented with R_{GEN} resistance. In this case supply circuit is photovoltaic module.

Depending on the duty factor, load and switching frequency, the converter can operate in continuous current mode (CCM) or discontinuous current mode (DCM). In this application it works in CCM. This mode enables independent control of duty factor (D) and frequency (f_{sw}) of converter control signals.

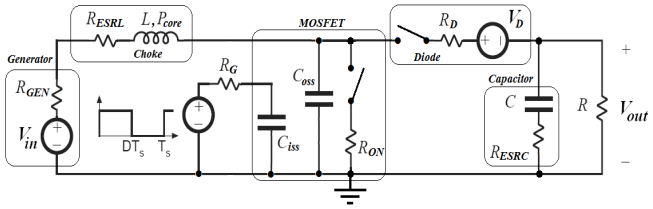

Fig. 2. Equivalent scheme of boost converter with parasitic elements [4]

A. Conduction losses

In order to determine the average power of conduction loss it is necessary to determine the effective current value through the parasitic resistance and the average current value through the voltage sources in boost converter model.

The average power of conduction losses in converter, when it operates in continuous mode, is equal to sum of average power in all elements, i.e.:

$$P'_{cond} = R_{GEN} \cdot I'^2_{Leff} + R_{ESRL} \cdot I'^2_{Leff} + R_{ON} \cdot I'^2_{TReff} + \\ + R_D \cdot I'^2_{Deff} + V_D \cdot I'_{Davg} + R_{ESRC} \cdot I'^2_{Ceff} \quad (2)$$

B. Dynamic losses

Dynamic losses in the converter consist of losses in choke core, transistor and diode. Dynamic MOSFET losses are losses in gate, output capacitance and losses which occur during switch mode change.

Power loss in the MOSFET gate is given follows as [5]:

$$P_{iss} = C_{iss} \cdot V_{cg}^2 \cdot f_{sw} \quad (3)$$

where C_{iss} is equivalent input capacitance of MOSFET, V_{cg} is supply voltage of gate control circuit and f_{sw} is switching frequency.

Power P_{oss} is power loss during the process of discharging the output capacitance C_{oss} of MOSFET, when MOSFET is turning on:

$$P_{oss} = \frac{1}{2} C_{oss} \cdot V_{Tr}^2 \cdot f_{sw} \quad (4)$$

where voltage V_{Tr} is equal to output converter voltage (Fig. 1).

Dynamic losses occur in transition process of switches. The average value of these losses can be shown as:

$$P_{Tsw} = k \cdot (t_{vr} \cdot I_{L\max} + t_{vf} \cdot I_{L\min}) \cdot V_{out} \cdot f_{sw} \quad (5)$$

where t_{vr} and t_{vf} are voltage rising and falling time respectively. Constant k is in the range between 1/6 and 1/2 [6].

Transistor dynamic losses, coming from diode recovery time, exist only when the converter operates in continuous mode and can be described as [7]:

$$P_{Tdiode} = V_{out} \cdot (I_{L\min} \cdot t_{rr} + Q_r) \cdot f_{sw} \quad (6)$$

where: V_{out} – output voltage of boost converter, t_{rr} – diode recovery time, Q_r – accumulated charge in pn junction area. These losses occur during switching of the transistor, when diode continues to conduct in opposite direction until the Q_r is discharged.

Choke core losses are due to hysteresis and eddy currents. To calculate the losses in the core, with sufficient accuracy, following relation can be used [8]:

$$P_{core} = k \cdot f_{sw}^{\alpha} \cdot \Delta B^{\beta} \cdot V_{core} \quad (7)$$

where V_{core} is volume of choke core, k, α, β are coefficients that can be found in technical specifications of core

manufacturers, while ΔB is maximum induction in the core.

Total switching losses are equal to the sum of individual switching losses of converter elements and they can be expressed as follows:

$$P_{din} = P_{iss} + P_{Tsw} + P_{oss} + P_{Tdiode} + P_{core} \quad (8)$$

Relations (8) shows that the switching losses in semiconductor elements are function of switching frequency.

III. Control Module With Fuzzy Controller

The control module regulates operation of boost DC/DC converters. It is based on fuzzy controller. This controller controls duty factor and frequency of converter control signals, pulse-width modulated (PWM) signals. In this way two important functions are realized. One is control of converter input voltage, so the MPPT algorithm is realized. This is achieved by duty factor control. The second is maximum efficiency of the converter, what is achieved by control of switching frequency (Eq. 8). So, fuzzy controller has two inputs and two outputs. One input is output power of solar panels and second is power losses of DC/DC converter. Outputs are duty factor of converter control signals and second is switching frequency. Block diagram of the realized control module is shown in Fig. 3.

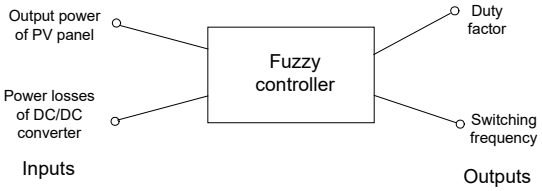

Fig. 3. Block diagram of the realized control module

A. Implementation of MPPT algorithm

Solar panels are current sources, whose output current and voltage, and on that way the power depend from many factors, among which the most important are temperature and intensity of solar radiation.

The dependence of the solar panel output power from its voltage is nonlinear. This dependence, for different values of temperature and solar radiation intensity, is shown in Figures 4. and 5. Taking into account the low efficiency of solar panels, it is very important control the panel output voltage so the maximum output power is achieved.

For the realization of MPPT algorithm simple fuzzy controller is used (Figure 3). One input in the fuzzy controller is difference of two successive samples of solar panel output power

$$\Delta p_{po}(n) = p_{po}(n) - p_{po}(n-1), \quad (9)$$

where $p_{po}(n)$ is solar panel output power in moment nT_1, and T_1 is time interval between two successive samples of the panel output power. Output from the fuzzy controller is change of solar panel output voltage ΔV_{po}.

Sign of ΔV_{po} is determined based on panel output voltage. If ΔV_{po} increases, sign of ΔV_{po} is retained. Otherwise, the sign is opposite

$$\operatorname{sgn}\left(\Delta\left(V_{pn}(n)\right)\right) = \begin{cases} \operatorname{sgn}\left(\Delta\left(V_{po}(n-1)\right)\right) & \text{if } p_{po}(n) \geq p_{po}(n-1) \\ -\operatorname{sgn}\left(\Delta\left(V_{po}(n-1)\right)\right) & \text{if } p_{po}(n) < p_{po}(n-1) \end{cases} \quad (10)$$

where $\Delta V_{po}(n)$ is change of panel output voltage in the moment nT_1.

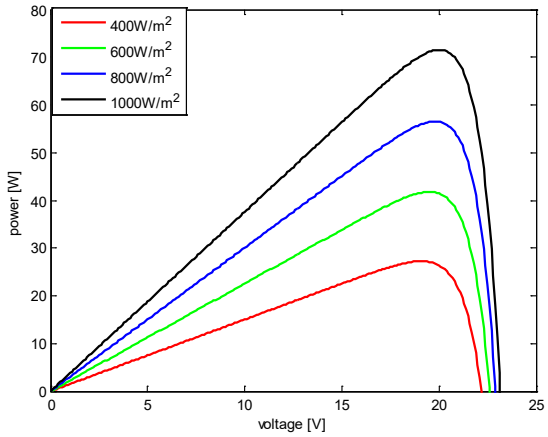

Fig. 4. Output power of solar panel in a funcion of panel voltage for different values of solar radiation

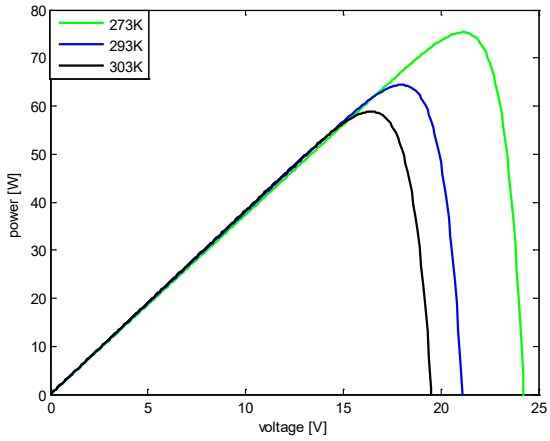

Fig. 5. Output power of solar panel in a funcion of panel voltage for different ambient temperatures

From the obtained values for the panel output voltage (input voltage of the boost DC/DC converter), new value of duty factor is determined

$$D(n) = 1 - \frac{v_{po}(n)}{V_{co}}, \quad (11)$$

where $D(n)$ is duty factor of boost DC/DC converter

control signals in the moment $nT1$ and V_{co} is converter output voltage.

B. Efficiency optimization of boost converter

Algorithm for efficiency optimization of boost DC/DC converter is realized as search algorithm with fuzzy controller. Boost converter efficiency for given operating conditions (input power and output voltage) can be optimized by adjusting switching frequency what is discussed in Section 2. Changing the switching frequency must not be disturbed defined operating conditions of the converter relating to maximum change of choke current, maximum ripple of the output voltage and maximum induction in the choke core.

This algorithm works as follows. Power loss is calculated as difference between the input and output power of the converter

$$P_{cL}(n) = P_{ci}(n) - P_{co}(n), \tag{12}$$

where $P_{cL}(n)$ is converter power loss and $P_{ci}(n)$ and $P_{co}(n)$ converter input and output power respectively in the moment nT_1. The difference of two power loss successive samples is calculated as

$$\Delta P_{cL}(n) = P_{cL}(n) - P_{cL}(n-1), \tag{13}$$

If $\Delta P_{cL}(n)$ is negative, change of switching frequency (Δf_{sw}) has same direction. Otherwise, sign of Δf_{sw} is opposite

$$\operatorname{sgn}\left(\Delta\left(f_{sw}(n)\right)\right) = \begin{cases} \operatorname{sgn}\left(\Delta\left(f_{sw}(n-1)\right)\right) & \text{if } P_{cL}(n) \le P_{cL}(n-1) \\ -\operatorname{sgn}\left(\Delta\left(f_{sw}(n-1)\right)\right) & \text{if } P_{cL}(n) > P_{cL}(n-1) \end{cases} \tag{14}$$

Based on $|\Delta P_{cL}(n)|$, value of $|\Delta f_{sw}(n)|$ is determined in the fuzzy controller so the new value of switching frequency in the moment nT_1 is equal to

$$f_{sw}(n) = f_{sw}(n-1) + \operatorname{sgn}\left(\Delta f_{sw}(n)\right)\left|\Delta f_{sw}(n)\right|. \tag{15}$$

In this way the switching frequency is changed so the the inverter works with minimum power losses for a given working conditions.

IV. Simulation Results

Simulations of described solar system are implemented in MATLAB. Simulation results which show the performance of the described MPPT algorithm are shown in the Fig. 7. and 8. It is assumed that there is a linear and step change of the parameters that have the most important impact to the characteristics of the PV panels, temperature (T) and solar radiation intensity (χ) (Fig. 6). Fig. 7. shows the output voltage, output current and output power for applied MPPT algorithm, and characteristics of temperature and solar radiation intensity shown in Fig. 6.

Graphics of PV panel output power for applied MPPT algorithm and for constant output voltage V_{po}=0.7V_{oc} with specified operating conditions (Fig. 6.) are shown in Fig. 8.

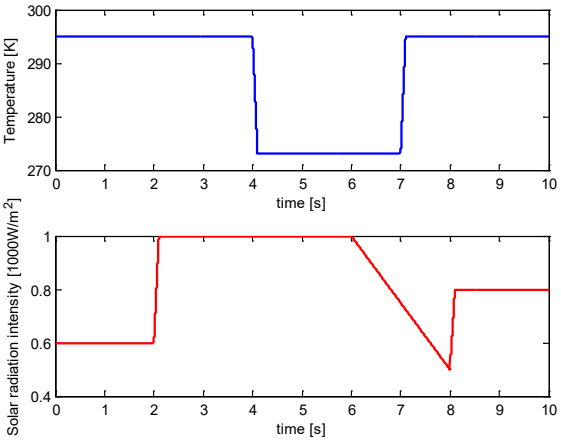

Fig. 6. Graphic of outside temperature and solar radiation intensity used in simulation

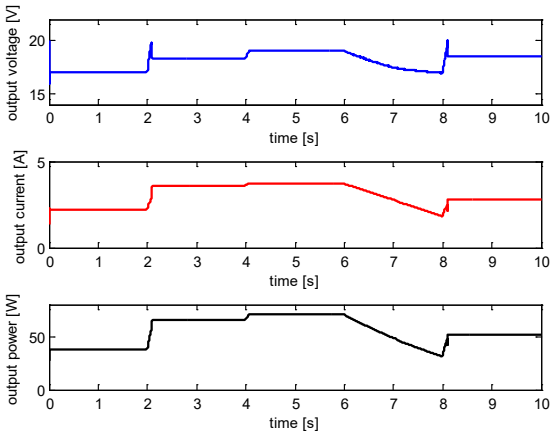

Fig. 7. Graphics of panel output voltage, output current and output power for applied MPPT algorithm based on fuzzy logic and the working conditions shown in Fig. 6.

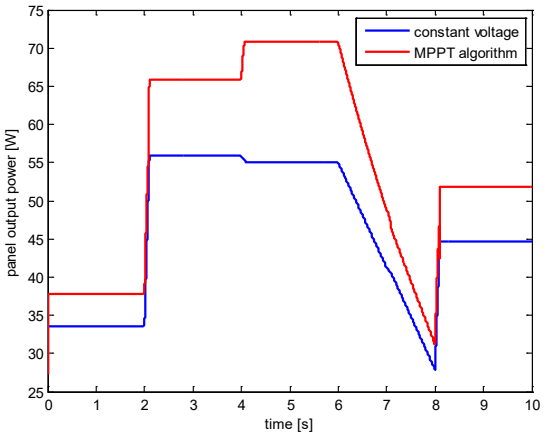

Fig. 8. Graphics of panel output power for constant voltage and applied MPPT algorithm and working conditions shown in Fig. 6.

Based on Fig. 7. and 8. it can be concluded that the proposed MPPT algorithm is fast and provides obtaining maximum power from the PV panel for given working conditions.

Operation of the controller in the efficiency increase of the applied boost DC/DC converter in the solar system has been tested through simulation. Obtained results are presented in Figs. 9 and 10.

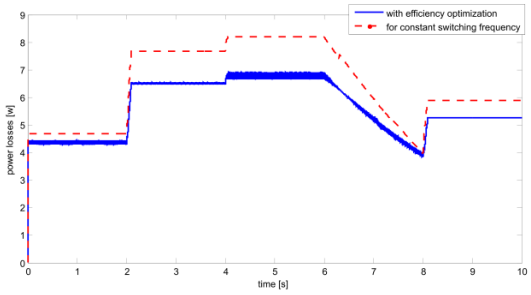

Fig. 9. Power losses for constant switching frequency and with applied efficiency optimization algorithm

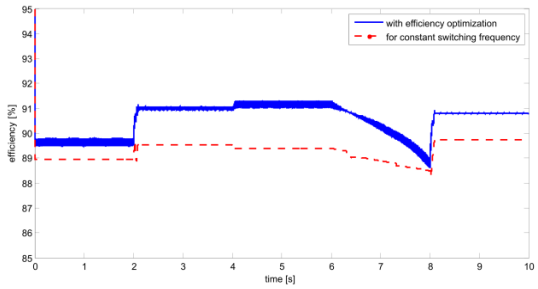

Fig. 10. Boost converter efficiency in observed solar system for for constant switching frequency and with applied efficiency optimization algorithm

Based on the results (Fig. 9 and 10), it can be concluded that the algorithm adjusts the switching frequency to the load. In this way switching losses are reduced and efficiency increased. These results correspond to the theoretical analysis in Section 2.

V. Conclusion

In this paper is presented a system which consists of photovoltaic panels, a DC/DC boost converter and a variable resistive load.

The control circuit is realized with fuzzy controller which controls duty factor and a switching frequency of the converter.

The following results have been achieved:

- Maximum utilization of available power from the PV panels (Figs. 7 and 8)
- Operation of the DC / DC converter with a switching frequency which provides maximum efficiency for a given working conditions (Figs. 9 and 10).

The system is modeled and tested in the MATLAB/Simulink.

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Modelling SAR of Mobile Phone Inside User' Head

Dejan Jovanović, Vladimir Stanković, Dejan Krstić, Nenad Cvetković

Abstract - This paper represents distribution of electric field which obtained inside a human head from source of electromagnetic radiation, i.e. the mobile phone. Also Specific Absorption Rate (SAR), within a user' head due to exposure to electric field from mobile phone was presented. For this research different models of human head were used. The first model was created as a phantom model, second one was created as model with a few layers (multilayers model) and the last one was created as a realistic model of head with all actual biological tissues and organs. In every case simulations were performed for the frequency of 900 MHz, which are the most common used in mobile communications. The parts of the human head are based on their electromagnetic properties (conductivity, electric permittivity, and magnetic permeability). In order to obtain the electric field distribution and SAR within head, the numerical calculation based on the Finite Integration Technique (FIT) and Finite Element Method (FEM) was performed.

Keywords - Nonionizing radiation, Electric field, Specific Absorption Rate, Finite integration technique, Finite element method.

I. Introduction

In order to make our everyday life more comfortable, various wireless devices used for transfer of different multimedia content and for regular daily activities at home have been developed. The common characteristic of all such devices is that they are sources of electromagnetic radiation.

The main expansion of mobile device use turned the focus towards the research of microwave impact on the human body for the purpose of assessing human health risk.

Compared to base stations located far from humans, mobile phone is source of electromagnetic (EM) radiation located close to the human head or body.

Such intense use, mostly among the younger population, can cause concern about health effects. In order to obtain relevant data, it is necessary to perform continuous research of the effects of EM radiation on human health.

In order to obtain the most realistic results of EM field distribution and values of SAR, we made a 3D human head model with size which corresponds of an average person and which consists actual biological tissues and organs.

Because of that it was necessary to make a model that would represent the human head structure as truly as possible (Fig. 1). [1, 2, 3, 4]

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This paper presents the distribution inside the human head of an EM field originating from mobile phones for operating frequency of 900MHz.

II. Electromagnetic Properties of Tissues

In order to describe the characteristics of biological tissue, it is necessary to define features that are as close as possible to the actual tissue. The real biological tissues are nonhomogeneous, nonlinear, and dispersive. Since the human body consists of different organs, each of the organs or tissues has to be described by adequate electromagnetic parameters that are used for biological tissues.

TABLE I
Electromagnetic Properties of model A and model B for $f = 900\text{MHz}$

Tisuue	ε_r	σ (S/m)	ρ (kg/ m^3)	Heat Capacity (kJ/kgK)	Thermal conductivity (W/m°C)
Cortical Bones	12,45	0,143	1850	1,313	0,32
Brain	45,805	0,7665	1030	3,630	0,51
Cerebrospin Fluid	68,60	2,410	1007	4,096	0,57
Fat	11,30	0,109	1020	2,348	0,21
Cartilage	42,70	0,782	1100	3,568	0,49
Pituitary Gland	59,70	1,040	1053	3,687	0,51
Spinal Cord	32,50	0,574	1075	3,630	0,51
Muscle	55,00	0,943	1040	3,421	0,49
Eyes	49,60	0,994	1060	3,615	0,53
Skin	41,40	0,867	1100	3,391	0,37
Tongue	55,30	0,936	1090	3,421	0,49
Teeth	12,50	0,143	2180	1,255	0,59

TABLE II
Electromagnetic Properties of model C for $f = 900\text{MHz}$

Tissue	ε_r	σ(S/ m)	ρ(kg/m3)
Shell	45.5	0,0016	1100
Fluid	41.4	0.145	1000

The influence of the dispersive characteristic is eliminated with the electromagnetic characteristic of tissues at a certain frequency. The following electromagnetic

parameters have to be correctly defined for every organ: electric conductivity, permittivity, heat capacity, density and thermal conductivity. For model A and model B which consist a different biological organs and tissues, the values of electromagnetic parameters are given in Table I. while the values of electromagnetic parameters for model C (phantom model) are given in Table II. [5] The proper boundary conditions at separation areas of the domains that connect individual organs have to be taken into consideration (model A and Model B).

III. Numerical Models of Human Head

Modeling of 3D models (Model A, Model B and Model C) was performed in two stages. First external look of models (Fig.1) and every tissues and organs was created in 3D Max Studio [6]. The second step was creating full model with actual tissues and organs and connecting certain electromagnetic properties with adequately tissues and organs (Table I and Table II) by using software package CST Microwave Studio [7]. The same software has been used for simulation of electromagnetic field and its influence on human head. Numerical calculation method which is used in this software is based on the Finite Integration Technique [8].

External look, horizontal and vertical cross-section with actual tissues and organs are shown in Fig. 1 and Fig. 2.

When using FEM analysis software, the key step before any computations is to create the mesh of elements. Finer mesh means the greater number of elements and thus the results will be more accurate.

Model C was also created with the same size as Model A and Model B (Fig. 1 and Fig. 2) while the electromagnetic characteristics of tissues were modeled only with two layers. Model B (phantom model) contains only two layers with electromagnetic properties as shown in Table II.

For this research actual smart phone (Fig. 3) has been used as a source of electromagnetic radiation. The current mobile phone consists of following parts: planar inverted F antenna (PIFA), display and mobile housing. The planar inverted F antenna (PIFA) as a source of electromagnetic radiation was modeled for the frequencies of f=900MHz as one of most common used frequency in telecommunication system, with power of P=1W [9] and impedance of Z=50Ω.

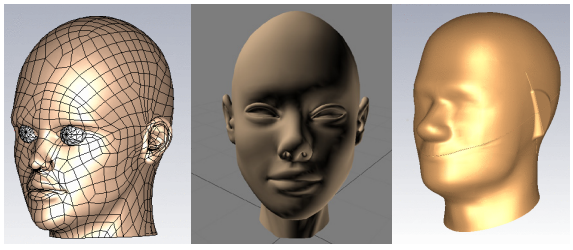
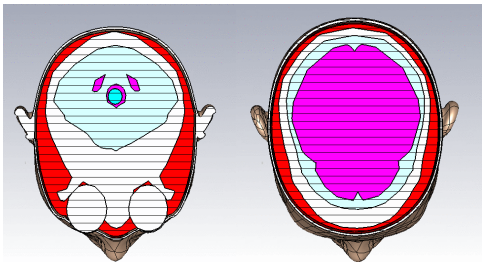
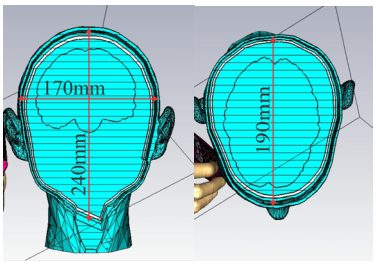


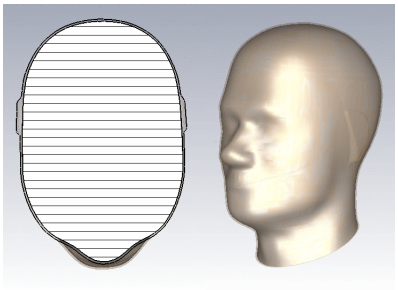
Fig. 1 - External looks of human head models: A-Realistic Model, B-multilayers Model and C-Phantom Model.



Model A



Model B



Model C

Fig. 2 – Horizontal and vertical cross-sections of the models with organs and tissues

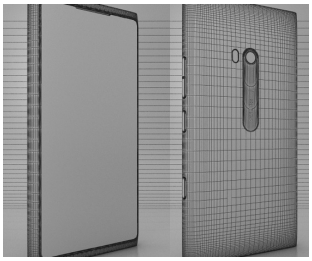


Fig. 3 - Model of actual smart phone

IV. Results

A. Electric Field Distribution

Calculation of the EM field in the head is based on the finite element method. The electromagnetic properties of head tissues for a 900MHz frequency are shown in Table I and Table II.

On the Fig. 4, in accordance with color at the surface of model we can observe that the greatest values of the electric field are just around the radiation source, where there is also the biggest influence of radiation and penetration of the electric field. The field decreases dramatically moving away from the source.

The Fig. 5. represent the maximum electric field distribution at $f = 900\text{MHz}$ for different models. Electric field levels are represented by different colours, whose values are shown by a colour palette on the right in each figure. Based on Fig. 5, (Model A, B and C) one can conclude that the envelope of electric field strength decreases with the distance from the area of field penetration into the head model. Therefore, the biological effects of radiation are more significant in the skin, subcutaneous fat tissue, head muscles, and the part of the brain closer to the radiation source.

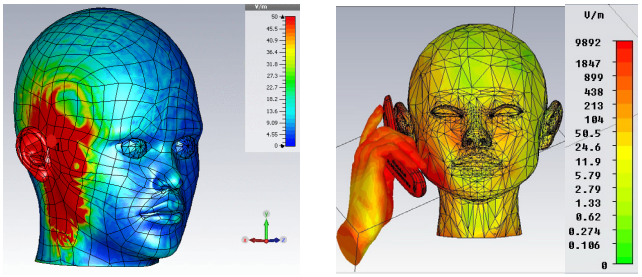
B. Specific Absorption Rate (SAR)

If biological tissue is in the path of EM wave propagation, the wave penetrates the tissue and a portion of the wave energy is absorbed in the tissue. A force affects the charged particles due to electric and magnetic components of the EM field. The internal energy increases and, consequently, the temperature increases and thermal energy dissipates. The difference of input and output wave energy at the boundaries of an object represents absorbed energy. The SAR quantity has been introduced to precisely define absorbed energy.

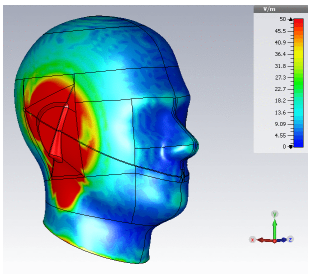
SAR is the power converted into heat in a body per unit mass, i.e.

$$\text{SAR} = \frac{P}{m} = \frac{\sigma E^2 V}{\rho_m V} = \frac{\sigma E^2}{\rho_m} \qquad (1)$$

This simulation represents the local SAR value in the human head (Fig. 6) which is calculated by using (1) for the frequency of 900MHz for Model A, Model B and Model C.

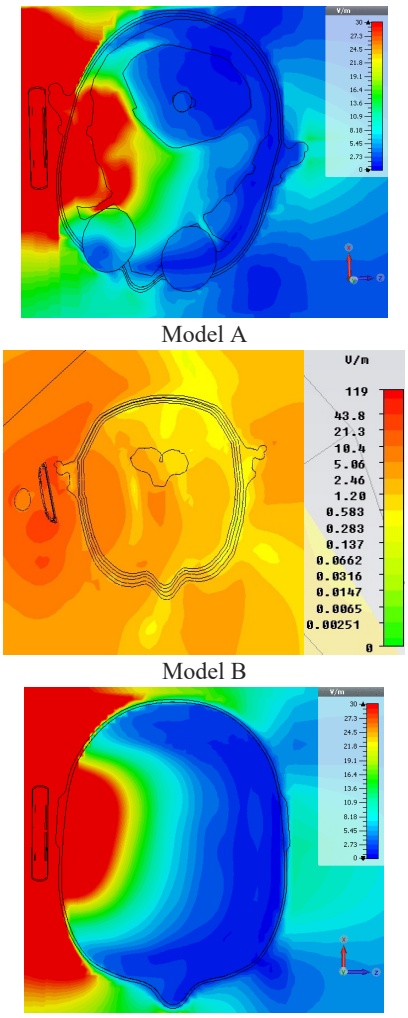


Model A Model B



Model C

Fig. 4 - The distribution of the electric field E [V/m] at the surface of human head models.

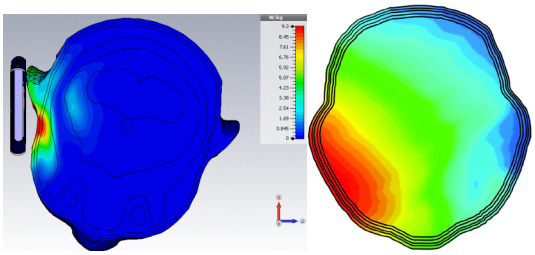


Model A

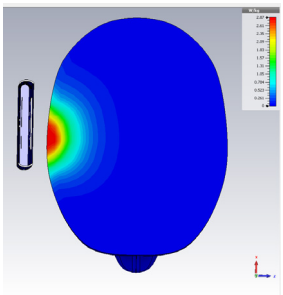
Model B

Model C

Fig. 5 – Electric field strength distribution inside human head



Model A Model B



Model C

Fig. 6. - SAR [W/kg] inside different models

Those results are obtained for output power of the mobile phone P = 0.25W. It should be noted that in the worst case for output power of P = 1W [10], values of SAR would be much greater than values shown in previously figures.

V. CONCLUSION

The aim of this study was to examine the influence of mobile phone radiation on human head by numerical calculation. To achieve this aim different models of human head have been used: realistic model with organs and tissues, multilayers model and phantom model with only two layers.

It was possible to graphically represent the features of electromagnetic wave penetration through the head models. Graphical representation showed the electric field strength distribution and SAR values in the human head for different models for frequency of 900MHz.

The results represent where the maximum value of absorbed energy is, how the field penetrates, and how much it weakens as the distance from the radiation source increases. Naturally, the highest radiation level is in the area next to the phone antenna, and it gradually decreases with every subsequent area.

The results for different cases of exposure showed disagreement between both the simulations used previously described models (Model A, Model B and Model C). In the case of a phantom model (Model C) can be seen from Fig. 5 that the penetration depth of electric field is deeper than in case with Model A and Model B (Fig. 5). This can be explained with higher volume of brain in case of phantom model and homogeneous characteristics of only one layer that supposed to simulate all biological tissue inside head.

More realistic and accurate results were obtained by using realistic model (Model A) due to this model is taking into consideration all biological organs and tissues with adequately electromagnetic properties (Table I). Because of these advantages of this Model A, its usage allows defining absorbed energy and electric field in each organs or tissues. This date can be used for medical purpose in order to describe dose and biological sensitivity of biological mater.

The realistic model (Model A) of human head provide exceptional assistance to researchers, with a new idea of connecting the simulation results obtained using this model the real structures of the human head, as shown in the paper.

ACKNOWLEDGEMENT

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Outage Probability of SC Receiver Operating in Both Microcell and Picocell Environment

Aleksandra Panajotović and Dragan Drača

Abstract - In this paper, the outage probability of selection combining (SC) receiver operating in different channel models, developed within IEEE 802.11n standard, is simulated. The presented results show in which extent an environment and a diversity influence on the outage performance of consider system.

Keywords – Diversity system, Outage probability, Simulation, Space-time-frequency-selective fading channel.

I. INTRODUCTION

Multiantenna techniques can be divided into two categories: diversity techniques and spatial-multiplexing techniques. The first ones are based on receiving same information in the multiple antennas aiming to convert an unstable time-varying wireless fading channel into a stable additive white Gaussian noise (AWGN)-like channel [1]. That provides upgrading transmission reliability of wireless system without increasing transmission power. Among well known diversity techniques, selection combining (SC) has the least implementation complexity since it processes signal only from one of diversity antennas, which is selectively chosen, and no channel information is required. Normally, the SC receiver selects the antenna with the highest signal-to-noise ratio (SNR) or, equivalently, with the strongest signal assuming equal noise power among the antennas [2].

The set of metrics, used to estimate the performance of wireless system, can be roughly divided into two groups: first-order and second-order performance metrics. First-order performance metrics are: outage probability (OP), error probability, system capacity, average output signal, etc. Second-order performance metrics are important for an adaptive system in which first-order metrics do not provide enough information for the overall system design and configuration. Average level crossing rate (LCR) and average fade duration (AFD) are second-order performance metrics [3]. It is obviously that the application and other aspects of consider system dictate which performance metric is the most important for analysis. However, the OP has been traditionally the most common used performance metric and, moreover, it is necessary for evaluation of second-order performance metric.

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Depending on the wireless environment, an appropriate statistical model can be used to describe fading behaviour in a channel. For example, the Rice model is adequate for the propagation consists of one strong direct line-of-sight (LOS) component and many random weaker components, while the Rayleigh model can be used when the LOS component does not exist. The advance of the Nakagami-*m* model lays in control of the fading severity, from sever to light, adjusting parameter *m*. The Weibull model is applicable in both indoor and outdoor environments. The performance of SC receivers operating in previous mentioned environments are studied through simulation and numerical analysis in [4]-[7]. In this paper we go one step forward by considering the performance of SC receiver operating in stochastic Multiple-Input Multiple-Output (MIMO) channel suitable to IEEE 802.11n.

II. OUTAGE PROBABILITY

The OP is defined as probability that the instantaneous error probability exceeds a specified value or, equivalently, probability that the output SNR, μ, falls below a certain specified threshold, μ_{th}. Mathematically speaking [2], the OP is defined as

$$P_{out} = \int_0^{\mu_{th}} p_\mu(\mu) d\mu \tag{1}$$

and represents the cumulative distribution function of μ. The wireless environment, in which diversity receiver operates, is characterized through the probability density function of output SNR, i.e. $p_\mu(\mu)$.

It is known that numerical analysis is not only easy and time-unconsumed but accurate way to estimate the system performance too. On the other hand, simulation presents good way to confirm the accuracy of already obtained numerical results. Moreover, simulation can also be used with scientific modelling of system to gain insight into its functioning.

In this paper, the simple stochastic MIMO channel model, empirically validated for both picocell and microcell environments, is applied for a link simulation. The main strength of this MIMO model is that it relies on small set of parameters to fully characterize communication scenario. These parameters are: power gain of the MIMO channel matrix, two correlation matrices

describing the correlation properties of both ends of transmission link and the associated Doppler spectrum of the channel path. They all are extracted from measurement results [8].

The algorithm presented in Fig. 1 describes the process of modelling of L-branch SC receiver operating in environments compliant to IEEE 802.11n and the simulation of its outage probability.

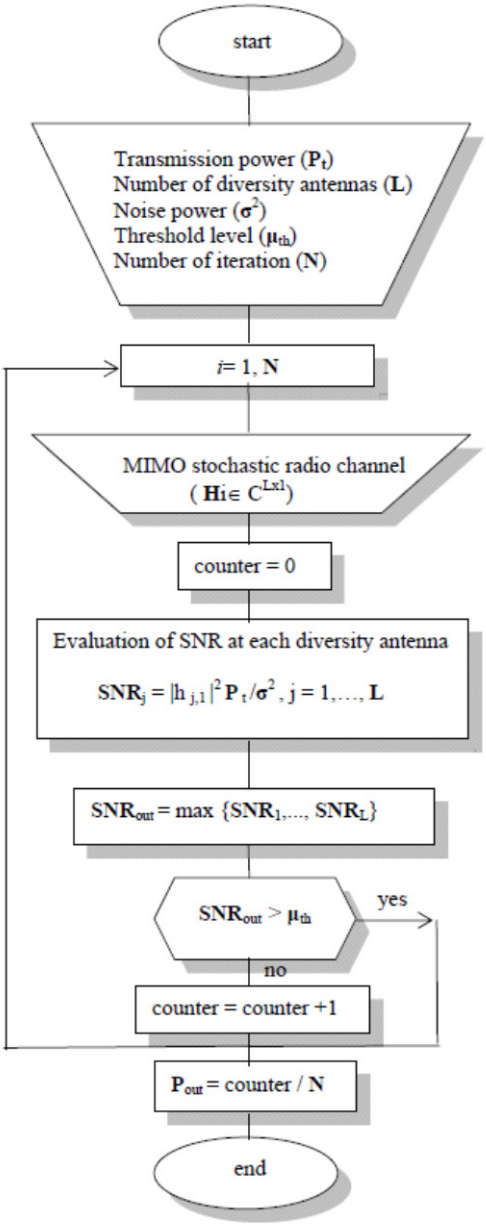

Fig. 1. Modelling and simulation of L-branch SC receiver.

III. Simulation Results

The figures presented in this section show simulation results of the OP of L-branch SC receiver operating in picocell (Fig. 2) and microcell environment (Fig. 3). The term picocell and microcell refer to indoor-to-indoor (E channel profile) and indoor-to-outdoor (B channel profile) [8]. Namely, B channel profile is indoor environment consists of small offices where distance between mobile station (MS) and base station (BS) is from 31 to 36 m with BS located outside. E channel profile is very large open area as airports or modern open offices.

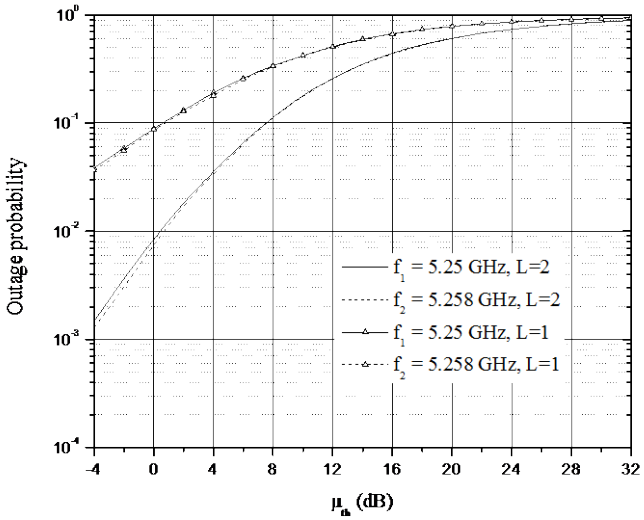

Fig. 2. Outage probability of dual SC receiver operating in picocell.

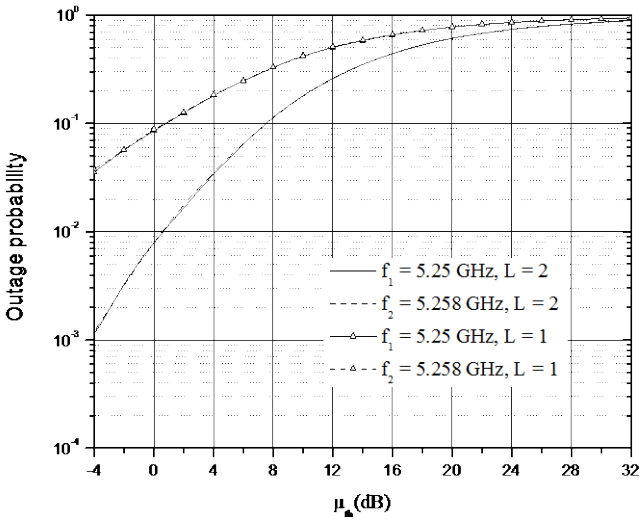

Fig. 3. Outage probability of dual SC receiver operating in microcell.

Figures 2 and 3 depict the OP versus SNR threshold. Note, in both figures there are outage probability curves for no-diversity and dual SC diversity systems evaluated for different frequencies. Since considered environments are compliant to IEEE 802.11n standard, carrier frequencies are $f_1 = 5.25$ GHz and $f_2 = 5.258$ GHz. It is obviously that B channel profile is not frequency-selective due to independence of outage system performance on the carrier frequency. Opposite to B channel profile, E channel profile is frequency-selective, especially for small threshold level, showing that for an orthogonal frequency division multiplexing (OFDM)-based wireless local area network (WLAN) system operating in this channel profile it have to be made difference between an antenna selection combining and a subcarrier selection combining, while it is not necessarily if the OFDM-based system operates in B channel profile. Moreover, SC system operating in small office experiences a bit better performance, i.e. less outage probability, than other one in large office. Note, the achieved diversity gain is independent on wireless environment, actually it provides same order-of-magnitude improvement of the outage performance.

IV. Conclusion

Since SC diversity technique is commonly adopted by WLAN systems [9], this paper presents simulation results for the outage performance of SC system operating in realistic, empirically validated, WLAN environment what emphasizes the contribution of presented results. This research can be extended to other performance metrics or other diversity techniques.

Acknowledgement

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LMS7002M FPRF 2x2 MIMO Transceiver IC With High Digital Content

Srđan Milenković

Abstract – This paper describes 2TX-2RX MIMO RF IC designed to support a variety of communication standards such as 2G, 3G, 4G and upcoming 5G applications. The chip itself is not particularly designed for those standards so it can be used in wide range of other applications. The chip has been manufactured in sub-micron CMOS technology, packaged in 261 pin aQFN 11.5x11.5 mm package. It is low power design hence typical power consumption is only 880mW in full 2x2 MIMO mode while the chip consumes 550mW in SISO mode.

Keywords – Field programmable RF, transceiver IC, MIMO, wireless communications.

I. Introduction

LMS7002M is a fully integrated, multi-band, multi-standard RF transceiver IC [1] that is highly programmable. It combines Low Noise Amplifiers (RXLNA), TX Power Amplifier Drivers (TXPAD), receiver/transmitter (RX/TX) mixers, RX/TX filters, synthesizers, RX gain control, TX power control, the analog-to-digital and digital-to-analog converters (ADC/DACs) [2][3] and has been designed to require very few external components.

The IC key features are summarized below.

- Field Programmable Radio Frequency (FPRF) chip.
- Dual transceiver ideal for MIMO.
- Continuous coverage of the 100 kHz - 3.8 GHz RF frequency range.
- Programmable RF modulation bandwidth up to 160 MHz using analog interface and up to 60MHz using digital interface.
- Supports both TDD and full duplex FDD.
- Transceiver Signal Processor block employs advanced digital techniques for enhanced performance.
- Low voltage operation, 1.25, 1.4 and 1.8V. Integrated LDOs to run on a single 1.8V supply voltage.
- On chip integrated microcontroller for simplified calibration, tuning and control.
- Integrated clock PLL for flexible clock generation and distribution.
- User definable analog and digital filters for customised filtering.

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Typical applications that LMS7002M has been used so far are:

- Broad band wireless communications.
- GSM, CDMA2000, TD-SCDMA, WCDMA/ HSPA, LTE.
- IEEE® xxx.xxx radios.
- WiFi operating in the Whitespace frequencies.
- Software Defined Radio (SDR).
- Cognitive Radio.
- Unmanned Aerial Vehicle (UAV).

Sections II, III and IV describe circuit functionality while section V presents the most interesting measured performances of the chip

II. Analog and RF Blocks

The top level architecture of LMS7002M transceiver is shown in Figure 1. The chip contains two transmit and two receive chains for achieving a Multiple In Multiple Out (MIMO) platform. Both transmitters share one PLL and both receivers share another. Transmit and receive chains are all implemented as zero Intermediate Frequency (zero IF or ZIF) architectures providing up to 160MHz RF modulation bandwidths (equivalent to 80MHz baseband IQ bandwidth). For the purpose of simplifying this document, the explanation for the functionality and performance of the chip is based on one transmit and one receive circuitry, given that the other two work in exact the same manner.

On the transmit side, In-phase and Quadrature IQ DAC data samples, from the base band processor, are provided to the LMS7002M via the LimeLight™ digital IQ interface. LimeLight™ implements the JESD207 standard IQ interface protocol as well as de facto IQ multiplexed standard. JESD207 is Double Data Rate (DDR) by definition. In IQ multiplexed mode LimeLight™ also supports Single Data Rate (SDR). The IQ samples are then pre-processed by the digital Transceiver Signal Processor (TSP) for minimum analog/RF distortion and applied to the on chip transmit DACs. The DACs generate analog IQ signals which are provided for further processing to the analog/RF section. Transmit low pass filters (TXLPF) remove the images generated by zero hold effect of the DACs, as well as the DAC out-of-band noise. The analog IQ signals are then mixed with the transmit PLL (TXPLL) output to produce a modulated RF signal. This RF signal is then amplified by one of two separate / selectable power amplifier drivers and two open-drain differential outputs are provided as RF output for each MIMO path.

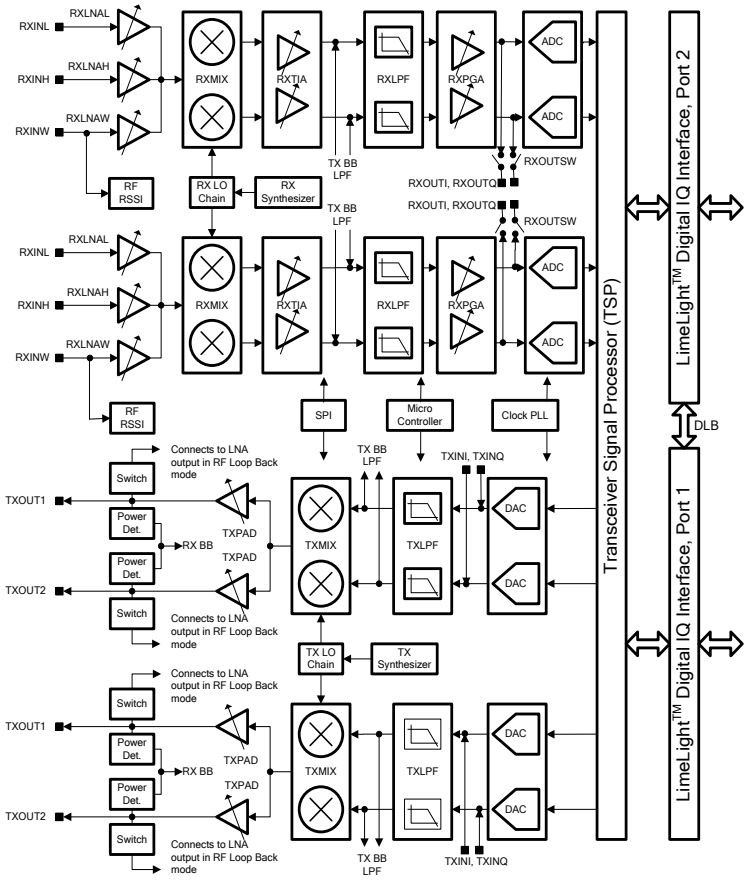

Figure 1: Functional block diagram

The LMS7002M provides an RF loop back option which enables the TX RF signal to be fed back into the baseband for calibration and test purposes. The RF loop back signal is amplified by the loopback amplifier in order to increase the dynamic range of the loop.

There are two additional loop back options implemented, one is an analog base band (BB) loop back and another is a digital loop back (DLB) as shown in Figure 1. The analog loop back is intended for testing while the DLB can be used to verify the LMS7002M connectivity to base band, FPGA, DSP or any other digital circuitry.

On the receive side, three separate inputs are provided each with a dedicated LNA optimised for narrow or wide band operation. Each port RF signal is first amplified by a programmable low noise amplifier (RXLNA). The RF signal is then mixed with the receive PLL (RXPLL) output to directly down convert to baseband. AGC steps can be implemented by a BB trans-impedance amplifier (RXTIA) prior to the programmable bandwidth low pass channel select / anti alias filters (RXLPF). The received IQ signal is further amplified by a programmable gain amplifier RXPGA. DC offset is applied at the input of RXTIA to prevent saturation and to preserve the receive ADC's dynamic range. The resulting analog receive IQ signals are converted into the digital domain with on-chip receive ADCs. Following the ADCs, the signal conditioning is performed by the digital Transceiver Signal Processor (TSP) and the resulting signals are then provided to the BB via the LimeLight™ digital IQ interface.

The analog receive signals can also be provided off chip at RXOUTI and RXOUTQ pins by closing the RXOUT switch. In this case it is possible to power down the on chip ADCs/TSP and use external parts which can be very useful for more resource demanding applications or where higher signal resolution is required. A similar option is also available on the TX side where the analog signal can be processed by external components. The on chip DACs/TSP can be powered down and analog inputs can be provided at TXINI and TXINQ pins.

Two transmitter outputs (TXOUT1, TXOUT2) and three receiver inputs (RXINL, RXINH, RXINW) are provided to facilitate multi-band multi-standard operation.

The functionality of the LMS7002M is fully controlled by a set of internal registers which can be accessed through a serial port and rapidly reprogrammed on the fly for advanced system architectures.

In order to enable full duplex operation, LMS7002M contains two separate synthesisers (TXPLL, RXPLL) both usually driven from the same reference clock source PLLCLK.

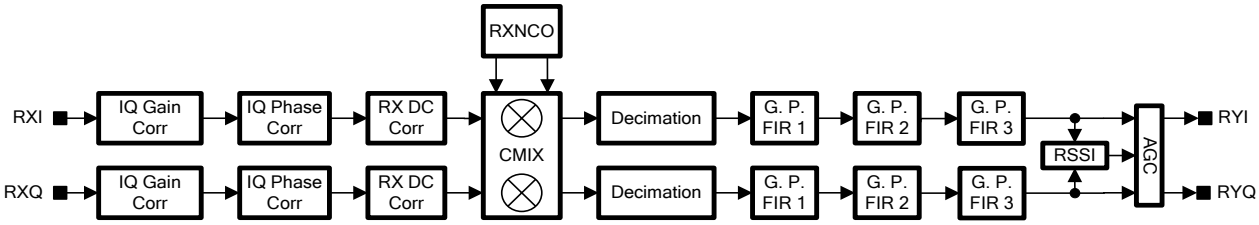

Figure 2: Structure of the RXTSP

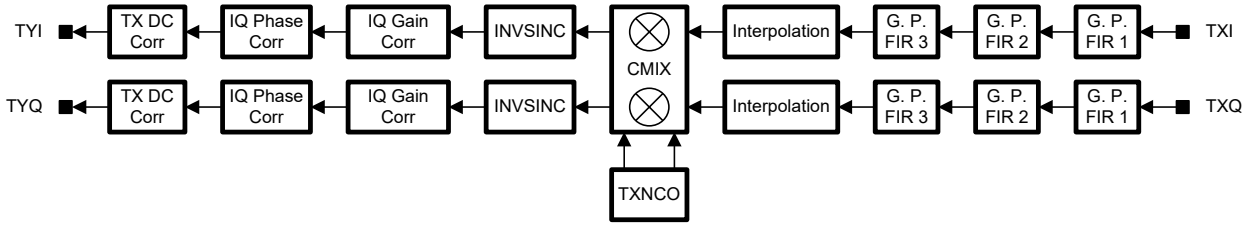

Figure 3: Structure of the TXTSP

III. Digital Transceiver Signal Processing Blocks

LMS7002M includes a high digital gate count within the Transceiver Signal Processor (TSP) block. The function of the TSP is to employ advanced digital signal processing techniques to enhance the performance of the analog/RF parts. This results in an improved performance of the overall system and a saving on total current consumption.

The TSP is placed between the data converters and the LimeLight™ digital IQ interface. Functionally, the RX and TX parts of the TSP are similar, as shown in Figure 2 and Figure 3, respectively.

In both the TX and RX TSP blocks there are three general purpose finite impulse response (FIR) filters, G.P. FIR 1, G.P. FIR 2 and G.P. FIR 3. The filter coefficients are fully programmable and the implementation does not force their impulse response to be symmetrical.

On the TX side, one of these filters could be used as a phase equalizer, which is a requirement in some communication standards such as CDMA2000. Another can be used to flatten the amplitude response of the TXLPF while the third FIR could be used to further enhance the channel filtering function of the BB modem. If phase equalization is not required then one filter can be used to minimize group delay variation of the analog TXLPF.

Possible applications of the G.P. FIR filters on the RX side are similar. One could be used to minimize group delay variation of the analog RXLPF while another could help to improve RXLPF adjacent channel rejection performance.

The interpolation block within the TXTSP takes IQ data from the BB modem and increases the data sample rate. The advantages of having interpolation are as follows. For narrow band systems (GSM/EDGE) or even moderately broad band (WCDMA, CDMA2000) modulation standards, the BB modem does not need to interpolate IQ data to the target system clock. The base band can provide output data at a much lower sample rate saving on power at the digital interface. Having a low data rate interface also simplifies the PCB design. However, the interpolator block generates data samples at the system clock rate, so the DACs run at a high sampling rate. As the DACs are running at a high frequency, it means that the quantization noise is spread over a wider frequency range which results in a better overall SNR. Also, the image generated by the DAC zero hold effect is further away from the wanted signal hence the specification for the TXLPF can be relaxed.

The reason for having decimation in the RXTSP is similar to that of interpolation in TXTSP. The ADCs can run at high frequency, and the specification of the RXLPF used as an anti-alias filter in this case is relaxed, the G.P. FIR improves adjacent channel rejection and the decimation circuit reduces the received data sample rate before sending the data to the BB modem.

The two Numerically Controlled Oscillators (NCO) and digital complex mixer (CMIX) in the TXTSP and RXTSP paths enable the LMS7002M to run in low digital IF.

Inverse sinc filters (INVSINC) within the TXTSP chain compensate for sinx/x amplitude roll off imposed by the DACs themselves.

The Tx DC Corr block is used to cancel residual DC offset of TXLPF. It is also used to cancel TX LO leakage feed-through as mentioned earlier.

There are three sources of the DC component at the RX output. These are the residual DC offset of the RXPGA and RXLPF, RX LO leakage feed-through and second order distortion (IP2). The Rx DC Corr blocks compensate for all of these sources of offset. The block is implemented as a real time tracking loop so any change of the RX DC due to either the signal level change, or due to RX gain change as well as any temperature effect will be tracked and cancelled automatically.

The IQ Gain Corr and IQ Phase Corr blocks correct IQ imbalance in both TXTSP and RXTSP in order to minimize the level of unwanted side band (image) component.

The last stage in the RXTSP path is a digital implementation of an Adaptive Gain Control (AGC) loop. Assuming that the BB modem does not require 12-bit full scale ADC outputs, the digital AGC block can provide a certain level of automatic gain control before the BB involves RF and IF gain stages.

IV. Digital Interfaces and Control

A. LimeLight™ Digital IQ Interface

The LMS7002M implements LimeLight™ digital IQ interface to the BB modem. LimeLight™ can be configured to run in one of the following three modes:

- JESD207 mode
- TRXIQ double data rate (DDR) mode
- TRXIQ single data rate (SDR) mode

All three modes are capable of supporting both TDD and FDD operation. The data throughput of JESD207 and TRX DDR is high enough to connect to up to 2x2 MIMO BB modems.

B. Serial Port Interface

The functionality of the LMS7002M transceiver is fully controlled by a set of internal registers which can be accessed through a serial port interface. Both write and read SPI operations are supported. The serial port can be configured to run in 3 or 4 wire mode with the following pins used:

- SEN serial port enable.
- SCLK serial clock.
- SDIO serial data in/out in 3 wire mode, serial data input in 4 wire mode.
- SDO serial data out in 4 wire mode, don't care in 3 wire mode.

C. On Chip Microcontroller

The LMS7002M can be fully controlled by external BB/DSP/FPGA ICs using 4-wire or 3-wire serial port interface. The controlling processor needs to implement a set of calibration, tuning and control functions to get the best performance out of the transceiver. The on chip microcontroller unit (MCU) provides the option for additional control. This allows the LMS7002M to be independent of the BB/DSP/FPGA and off-loads these devices.

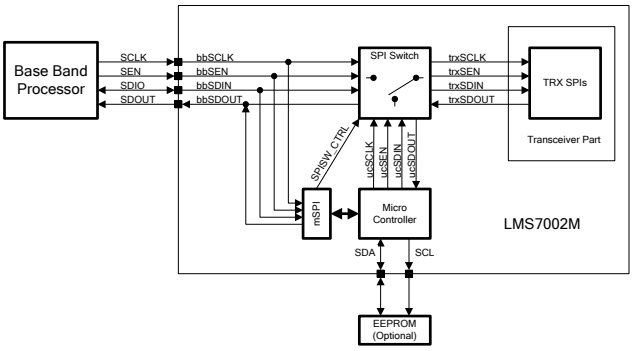

Figure 4: On chip microcontroller connection

MCU integration within the LMS7002M chip is shown in Figure 4. Since the chip communication to the outside world is done through SPI, the MCU uses the same protocol hence the block mSPI (master SPI) is placed in front of it. The MCU communicates to the transceiver circuitry using the same SPI protocol as the BB processor itself. This is implemented via ucSPI lines shown in Figure 4. There is two way communication between the MCU and BB via mSPI. The baseband can trigger different calibration/tuning/control functions the MCU is programmed to perform. The MCU reports a success, failure or an error code back to the base band processor.

In this architecture, the base band processor acts as master since it controls the whole chip, (transceiver as well as MCU). The base band processor also controls the SPI switch (via SPISW_CTRL control bit/line of mSPI) i.e. taking control over the transceiver part or handing it over to the MCU. The MCU acts as a slave processor. It can control the transceiver only if the base band allows that via the SPI switch.

MCU key specifications are as follows:

- 8-bit microcontroller.
- Industry standard 8051 instruction set compatible.
- Memory
  8 KB SRAM program memory
  2 KB SRAM working memory
  256 B dual port RAM
  All on chip, integrated.

D. Data Converters Clock Generation

The clock generation circuit for the data converters is shown in Figure 5. It shares the same reference clock input REFCLK with the RF synthesizers. The clock PLL then generates a continuous frequency range centred around 2.5 GHz. The feed forward divider (FFDIV) is programmable and capable of implementing division values $N = 2(n+1)$, $n = 0, 1, \ldots, 255$

There is a fixed divide by 4 within the ADC block hence clock division on the DAC side to provide more flexibility. There is a MUX to connect either Fpll, or Fpll/M to either ADC or DAC clocks. M is programmable and can be set to $M = 1, 2, 4$ or 8. The other CLKMUX

output will be connected to the other data converter clock input.

TSP blocks receive the same clock as the corresponding data converter, hence there is no need for complex non-power of two or fractional interpolation/decimation. TSP blocks have programmable interpolation/decimation and generate MCLK clocks going back to the base band processor via the LimeLight™ port.

The circuit implements a continuous clock frequency range from 5 MHz to 640 MHz for the data converters.

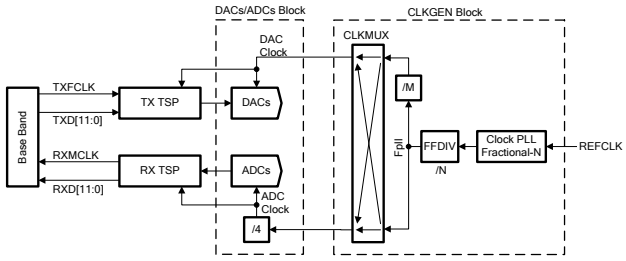

Figure 5: Clock generation and distribution

E. Calibration and Initialization

There are a number of calibrations which the LMS7002M can carry out internally when instructed via the SPI. These calibrations can be initiated on power up/reset to produce optimum settings. Initialization and calibration steps are summarized below.

Initialization

- Power up the chip. In case of using multiple off chip LDOs, power up sequence is not important.
- Apply RESET pulse (active low). This sets all the configuration registers to their default values.
- Overwrite some registers defaults if required.

Available calibration options and recommended order of execution

- TX, RX and clock synthesizer VCO tuning.
- TX and RX analog LPF pass band tuning.
- RX DC offset and RX LO leakage cancellation.
- TX DC offset and TX LO leakage cancellation.
- TX IQ imbalance calibration.
- RX IQ imbalance calibration.

V. Measured Results

Pass band of both transmit and receive analog filters is fully programmable and is tunable up to 80 MHz. Figure 6 illustrates selectivity and tunability of LMS7002M analog filters. This figure shows only low band section of RX filter as an example. Other filters response is similar with the difference that high band sections extend tunability up to 80MHz.

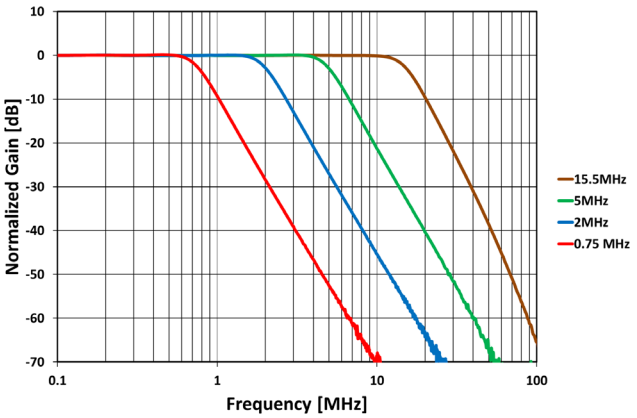

Figure 6: Analog RX LPF amplitude response

LMS7002M transmit output power versus frequency is plotted in Figure 7. Both TX outputs (TX1 and TX2) are measured with obviously different matching networks.

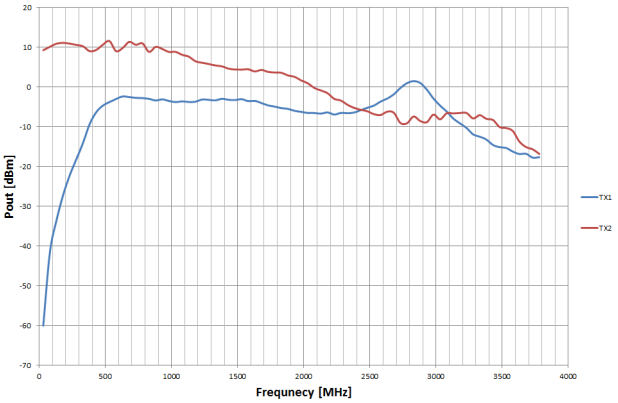

Figure 7: Transmitter gain versus frequency

LMS7002M receiver gain versus frequency is shown in Figure 8. All LNA inputs (LNAH, LNAL, LNAW) are measured. As in the case of the TX chain, different matching networks are used for three RF receiver inputs.

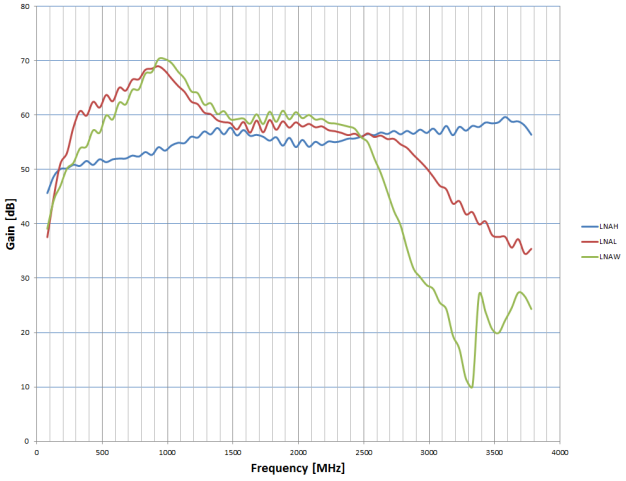

Figure 8: Receiver gain versus frequency

Continuous wave (CW) is used as test signal while measuring TX and RX gain. Figure 7 and Figure 8 show that with proper matching and selecting suitable RX RF input/LNA, LMS7002M provides excellent wide frequency range of operation.

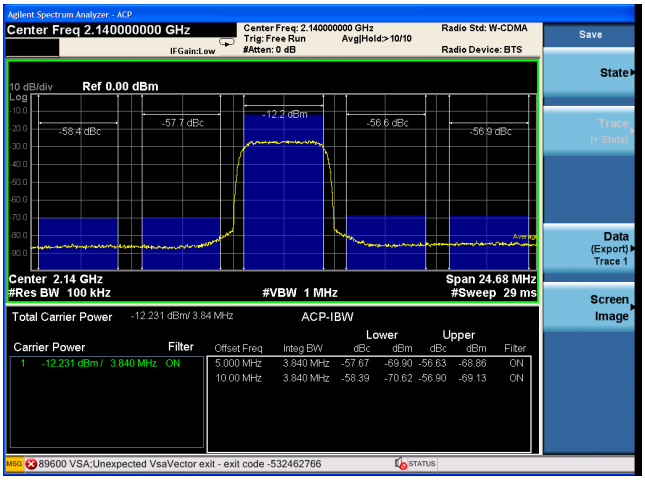

Figure 9: ACPR at 2.14GHz

Adjacent Channel Power Ration (ACPR) is measured using single carrier WCDMA modulated test signal where RF LO is the middle of Band I up link (2.14GHz). Result is shown in Figure 9. Measured ACPR is -56dBc which well over perform the number required by 3GPP standard itself (around -45dBc).

Error Vector Magnitude (EVM) is measured using very demanding 20MHz wide LTE modulated signal. As Figure 10 shows, measured EVM is 1.25% which again outperforms EVM requirement of 3GPP standard (around 8%).

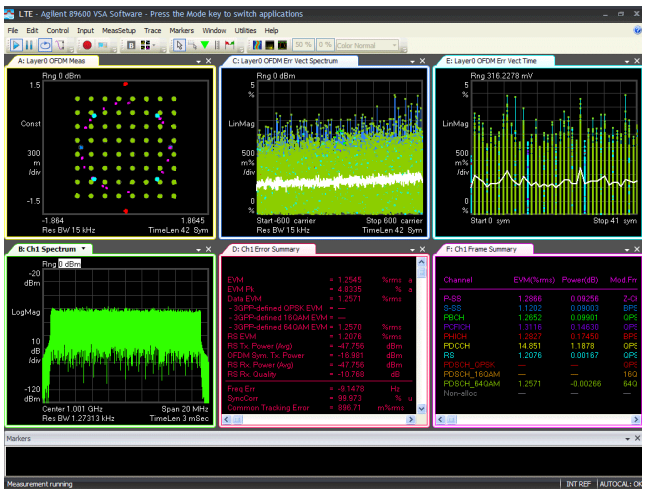

Figure 10: EVM at 1GHz

VI. Conclusion

Very flexible low power MIMO RF IC (LMS7002M) is described in this paper. Measured results show wide frequency range operation of the chip. Also the chip outperforms most of the major communication standards in terms of transmit spectrum mask (ACPR) and modulation accuracy (EVM) leaving excellent margin for the external PA to contribute while still keeping the whole system within the specifications.

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Improving HDL Higher Level Logical Analysis Using Boolean Function Feature

Vladimir Zdraveski, Andrej Dimitrovski, Dimitar Trajanov

Abstract — Increased designers' interest in digital system design using hardware description languages has resulted in a huge data set of open source, available on the Web. Difficulties in discovering specific component introduce the need of automation in the process of search and reuse of already existing components. Despite the interface, a very important part required for a complete automation is the software analysis of the components' inner architecture. Applying the Semantic Web methodologies and using our existing hardware description ontology, we propose extension that will enable a semantic annotation of the inner architecture and will significantly improve the tools for automatic search and system composition of existing components. The ontology is published and can be used as a model for a standardized annotation, in order to increase the availability of the existing components and to provide easier reuse in novel designs. The concept is also applicable inside a company, to accelerate the retrieval through the local repositories of components.

Keywords — architecture, design reuse, linked data, ontology, system on chip.

I. Introduction

Hardware description languages (HDLs) are mostly used during the chip production process [1][2][3], but recently many programmable chips are embedded in production version of systems [4], as peripheral data adapters or configured as co-processors that distribute the processing power and reduce the load of the central processor [5][6]. This new approach explores a new era for the higher-level programmers to put their own logic in the programmable chip, getting them much closer to the HDL perspective, which they found very complex to do it from scratch.

We are also aware that a large bundle of HDL code is already published to many public web repositories. There are many web portals [7] containing projects available under open licenses (GPL, Apache, etc.). Although portals offer a basic classification of projects, however, finding a specific component is still very difficult and slow. Portals have no possibility for flexible search (filter by ports, type of component and so on.).

Reasons for the lack of electronic design automation tools for sharing and reusing the HDL code may be identified in the problem complexity, which mainly arises from the point where a software tool should determine the inner architecture of an HDL component.

Applying the main idea of the Semantic Web [7] [8], we explore a new approach towards a more granular (deeper) annotation of the HDL code/components and a higher-level of semantic knowledge [9] retrieved from it. Hardware description language has a certain structure, so it is possible to make automatic semantic annotation using ontology and software that will generate semantic resources for digital circuits.

Identifying the possibility of applying Semantic Web tools for the design of digital systems [10], we have implemented an early version of the HDL IP Cores system [11]. It performs automatic semantic annotation only for the interface of the components. The system consists of a web application and client plug-in [11] for Eclipse. Web application contains a Web robot that searches and downloads HDL components from the web and then each component passes through a process of automatic semantic annotation. Generated meta-data is stored in a semantic database (repository; storage). The system performs deeper analysis and mutual comparison of components and enables their ranking according to similarity and compatibility with a particular component. Client plug-in provides all functionalities of the system, directly into the designer's native development environment.

HDL IP Cores so far provide the automation in data collection and search functionality, but still there is a lack of deeper understanding of the architecture's type, which is crucial for any advanced search and component composition. Solving this problem, we have created a new module that will recursively annotate the instantiated components down to the level of basic logical blocks and thus retrieve the logical function of a given architecture. When available, the Boolean expression for a given architecture will be another property for component's matching and similarity determination process, leading to an improved EDA tool for sharing and reuse of existing HDL code.

II. Related Work

Semantic analysis of the logical circuit is extremely important in simulators and most of them provide many advanced functionalities. Among them, there is the working environment (desktop) Xilinx ISE with built in simulator ISim [12], which allows very precise and exact time execution of simulations, generating multiple ways of simulation (manual, graphically, through the terminal) and a range of formats in which you can save the result of the simulation. The simulator of Cadence [13] allows the verification, according to the well-known open methodologies OVM (en. "Open Verification Methodology") and UVM (en."Unified Verification Methodology"), enables fast and easy integration with various verification processes, as well as data level simulation (RTL), simulation of behavior, simulation with reduced consumption and etc. Some simulators [14][16] allow automated generation of test environments, using

ready generic libraries, which significantly accelerates the components testing process.

HADES [18] simulator is commonly associated with the academic environment and is considered as a tool for beginners. The capabilities of HADES [18] are quite open, as it is modular and provides an open application programming interface (API) in Java, which is a very good opportunity to exploit its internal logic for semantic execution of simulations. Additionally, it contains a module for integration with VHDL.

What is important to note is that simulators are developed primarily in order to provide time accuracy and in the precise execution of the given models than in the direction of automatic determination of the type of components and/or automatic composition and reuse systems. However, some of their functionalities is possible to be used to improve the semantic annotation of components architecture [11].

III. Boolean Function Retrieval Process

Automatic interface annotation of components allows a low level of semantic analysis. In order to enable fully automatic search and automatic composition of systems, a software must consider the internal architecture of the components.

The logical function retrieval process can be separated into two phases. The first phase is the automatic semantic annotation of the internal architecture, while the second phase is exploiting the obtained semantic resources into an unambiguous logical (Boolean) function, which describes the architecture. The two phases are actually interconnected so that the first phase is the tool for the second phase that defines the result.

In our case the first phase is done by the annotation module of the HDL IP Cores system and the internal architecture of components is modeled as interlinked instances of simpler architectures. This methodology of developing new architectures has been accepted in the paradigm of structured representation of architecture within the hardware description languages (HDL), such as VHDL.

The HDL IP Cores annotator is based on ontology [12] which represents a semantic structure of hardware. In the ontology we provide the necessary classes and relations for the full annotation of architecture which continues to be the main tool for semantic search, comparison and simulation of multiple digital components that are found and distributed all over the web. The annotator will also provide the architecture type (such as Gate, Multiplexer, Coder and etc.).

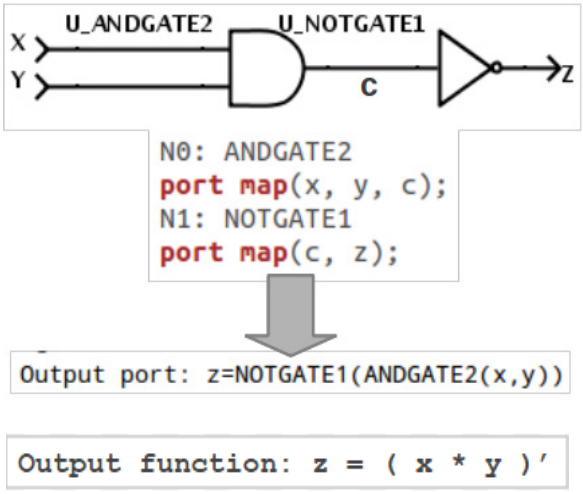

Fig 1: Annotation of logical function

The second phase will extract the logical function using semantic resources (RDF) which architecture is annotated with. The process of extracting the logical function of the architecture defined in VHDL is illustrated in Fig. 1. Architecture has an interface with two inputs (X and Y) and one output (Z). It contains an instance of "AND"-gate ("U_ANDGATE2") and an instance of a logical inverter ("U_NOTGATE1"), mutually interconnected with a signal "C". The part of the code that is instantiating the components are shown in Fig. 1, while the full content of the file is displayed in Appendix.

The final goal is to obtain the logical function of the output port "Z", i.e. to find the logical functions for all output ports of the architecture. The proposed algorithm for the logical function determination of the output port aims to find the input signals that function depends on, connecting recursively the inner instances and associated signals. The result of the algorithm is the architecture's logical function in Prolog syntax. The algorithm starts from each output port and is recursively finds component instances and its inputs, until the architecture inputs are found, Fig. 2.

The architecture description in the form of a logical function will be a good base to improve the algorithms and systems for automatic classification and composition of components, since it will allow unambiguous comparison of two architectures, according to the logical search function and appropriate ranking results according to mutual similarity and compatibility.

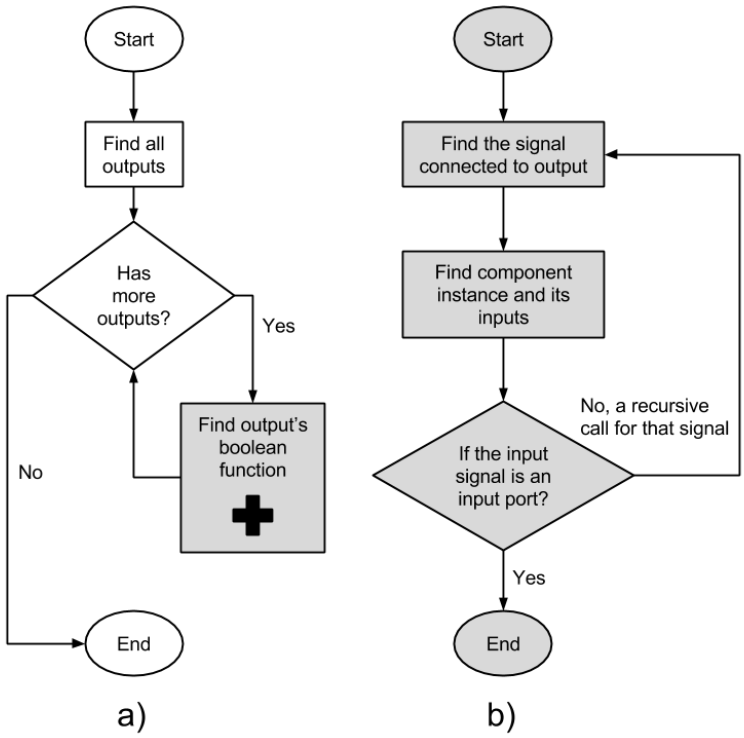

Fig. 2. Algorithm's flowchart. The algorithms are called for each output port (a) and for each output recursively finds component instances and its inputs, until the architecture inputs are found (b).

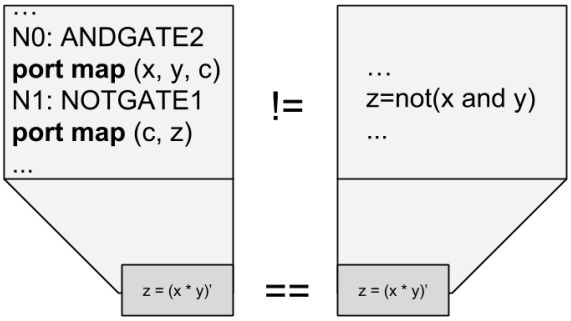

Fig. 3. Syntax abstraction layer. The VHDL codes of both components are different, but the Boolean functions are equal.

Thus, a level of syntax abstraction is introduced, as shown in Fig. 3, and different HDL IP Cores (even in different hardware description languages) may be compared and matched.

As already noted, the proposed algorithm works only for combinational circuits, whose architectures are described by structural paradigm. In case when using processes (functions) for definning the architecture of systems, the procedure for determining the logical function of architecture is significantly more complicated because the process would have to be modeled as a black box with a custom interface, and then to determine the type of architecture.

This procedure, is not possible without automatic execution of the simulation, except in the simplest scenarios. The procedure is also difficult to perform for sequential logic circuits, even the use of the simulator can not always be expected to lead to an unambiguous determination of architecture.

From the previous elaboration, the process determination of the logical function of combinational digital circuits described in hardware description languages is obvious that as the output receives the logical function output port "Z", from which could be easily obtained a mathematical function of the output "Z". That is equal to the negation of the product of inputs "x" and "y". This operation certainly belongs to the class of reverse engineering processes, since from an existing HDL code it obtains the mathematical function (expression), which might be used, elaborated, analyzed in different directions.

I. Future work

This paper illustrates the process of obtaining a logical function for combinational logical circuits described with structural paradigm, which is the first step in automatic semantic annotation of the internal architecture of digital systems.

Further step is to expand the procedure in order to cover the logical circuits defined by processes (functions). For this purpose, we will use the programming interface of the simulator HADES. Additionally, there is provided a library with classified components (gates, multiplexers, counters, etc.), which would be a good basis for algorithm training and automatic generation of rules for determining the architecture type of the new components.

Afterwards, unambiguous or using heuristic algorithms would be necessary to describe the architectures of complex sequential circuits and digital systems. This concept can encompass the most of the components available today and provide advanced functionalities within the HDL IP Cores system.

APPENDIX

```
library  ieee;
use  ieee.std_logic_1164.all;

entity NANDGATE2 is
    port(
        x : in STD_LOGIC;
        y : in STD_LOGIC;
        z : out STD_LOGIC
        );
end NANDGATE2;

architecture NANDGATE2 of NANDGATE2 is

signal c, d: std_logic;
   component NOTGATE1
       port(
           n_in : in STD_LOGIC;
           n_out : out STD_LOGIC
           );
   end component;

   component ANDGATE2
      port(
          a_in1, a_in2 : in STD_LOGIC;
          a_out        : out STD_LOGIC
          );
   end component;

   begin
   N0: ANDGATE2
      port map(x, y, c);
   N1: NOTGATE1
   port map(c, z);
end NANDGATE2;
```

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EASYSim: Energy-aware embedded system simulator

Strahinja Janković, Dragomir El Mezeni, Vladimir Petrović, Ivan Popović, Jelena Popović-Božović and Lazar Saranovac

Abstract - In this paper energy-aware embedded system simulator is presented. Simulation model supports describing behavior of different hardware and software subsystems and power and performance management algorithms. Using presented simulator, two algorithms with different optimization goals were tested: power management of single processor using Dynamic Frequency Scaling and multiprocessor Load Balancing. Presented simulator can be used for development of scheduling and power management algorithms, as well as power consumption estimation of embedded systems.

Keywords – Embedded systems, Multiprocessor, Power Management, Simulation.

I. Introduction

Power management is an important topic for modern embedded systems. It can be used to reduce cooling costs and electricity bills of stationary systems and prolong battery life of mobile systems. Power management techniques can be divided into static and dynamic. Static power management techniques are used to keep system that is idle in a power-efficient state, with System level suspend as an example. Dynamic power management [1] techniques are used on a component (or group of components) level and they work by keeping a component that is idle in a low power state, like clock and power gating, or by reducing performance if a component is not fully utilized, like Dynamic Voltage and Frequency Scaling, DVFS.

Modern embedded systems can be complex, having heterogeneous multiprocessor architecture [2], [3], and many different hardware accelerators and peripherals. Measuring power consumption of such system, or some part of the system, can be a challenging task. Also, because of fast development process of modern embedded systems performance and power consumption of such systems needs to be evaluated even before hardware prototypes for all components in the system are available.

On the other hand, simulated environment makes development easier, since it allows different aspects of the system to be modeled and system to be analyzed on different abstraction levels. It is much easier to develop new power management algorithms and evaluate power consumption of an embedded system in a simulated environment because it is easy to control testing conditions and to reproduce certain testing scenario. It is also easier to automate testing and analyze feasibility and performance before hardware is available.

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Different multiprocessor simulators have been previously developed. Many of these simulators are ISA-level simulators, which makes them too complex for describing and evaluating algorithms, or do not take power consumption into account. WSim [4] is an ISA-level simulator of MSP430 and ATMega microcontrollers, used for wireless sensor networks simulation. It is possible to evaluate energy consumption using WSim, but it is limited to only these two architectures. Gem5 [5] is an ISA-level simulator which supports several architectures (Alpha, ARM, SPARC and x86), with different levels of details and possibility to evaluate power consumption. Simics [6] is a full system simulator, which allows detailed simulation of hardware subsystems, but it does not take energy consumption into account. SimSo [7] is multiprocessor simulator used to evaluate multiprocessor scheduling algorithms, but it does not take energy consumption into account. STORM [8] is also multiprocessor simulator for scheduling algorithms evaluation and it takes energy consumption into account. Unlike previous works which aim at accurate ISA-level simulation or are focused primarily on multiprocessor scheduling algorithms, we propose the new multiprocessor Energy-Aware embedded SYstem Simulator (EASYSim) for development and evaluation of algorithms for performance and power management.

The rest of the paper is organized as follows. Key concepts and simulation model are defined in Section 2. Implementation details for one possible realization of defined concepts are described in Section 3. Functional verification of simulator is presented in Section 4 by detailed description of two common optimization scenarios: DFS of single processor and load balancing of multiprocessor system. Discussion and future perspectives are given in Section 5.

II. Simulation model

Key elements of presented simulator are simulation environment, engine and manager.

Simulation environment is collection of simulation objects. Every simulation object has following attributes: power consumption, execution time and synchronization interface. Simulation objects can have parameters which modify their attributes. For instance, objects that are used

to emulate hardware components can have performance in certain operating state (e.g. CPU frequency) as parameter that affects power consumption attribute, or latency caused by transitioning from one state to another as parameter that affects execution time. Also, objects that are used to emulate software components can have priority as parameter that affects synchronization interface. Simulation objects can be grouped to form complex objects and different dependencies among them can be defined.

Simulation engine is used to execute simulation. It is a discrete event simulator based on SimPy [9]. Simulation engine provides methods for synchronization and communication between objects.

Simulation manager is power and performance management algorithm. If this algorithm is implemented in software, hardware or combination of two, it contributes to the power consumption of simulated system as any simulation object. If simulation manager is an external influence, then its execution does not consume power.

Energy consumption of simulated system is obtained by summing energy consumption of each individual simulation object,

$$E_{SYS} = \sum_i E_{OBJi} \quad (1)$$

Total energy consumed by object OBJ_i is

$$E_{OBJi} = \sum_j P_j T_j \ , \quad (2)$$

where j represents a combination of OBJ_i parameters (e.g. frequency and supply voltage combination), P_j is average power consumption and T_j is time period while parameter combination j is active. Since simulation objects can be used to represent both software and hardware, power consumption needs to be defined for either of these, depending on available information. There should be no overlapping in power consumption definition, in order to obtain accurate measurements.

III. Implementation Example

In order to demonstrate how previously defined concepts can be used for realization of an evaluation system, example implementation that supports a CPU core model and program task as simulation objects was created.

A. CPU core model

Implemented CPU core model has following parameters: frequency and latency. Both parameters are provided as discrete values. For easier management, active and inactive power states are introduced [10] (Fig 1.). Power consumption is given for each individual state. Active power states have non-zero frequency and inactive power states have non-zero latency. Also, idle state is defined which has both frequency and latency equal to zero. Since CPU power consumption depends on utilization, this is modeled by calculating average of energy spent in active and idle state. If processor spends T_{A0} time in active state A_0 and time $T - T_{A0}$ in idle state, power consumed during time period T can be calculated as

$$P = \frac{P_{A0}T_{A0} + P_I(T - T_{A0})}{T} = P_I + \frac{T_{A0}}{T}(P_{A0} - P_I) \quad (3)$$

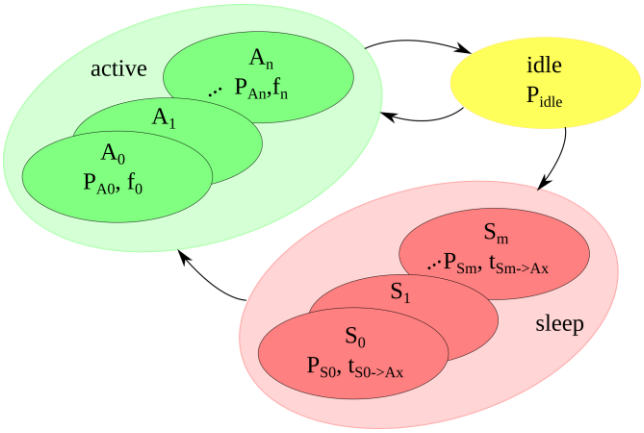

Fig. 1. CPU core state machine

Idle state is entered every time CPU core has no program load. Interface for triggering frequency change and transitioning into low power state is provided. CPU core is single-threaded and supports external interrupt handling. Each CPU core has unique ID.

Power model, i.e. list of supported power states for a CPU core is configured using a JSON file (Fig 2.).

```
{
    "cpu0": {
        "active": [{
            "id": 0,
            "name": "p0",
            "power": 120,
            "frequency": 5
        }],
        "idle": [{
            "id": 0,
            "name": "idle",
            "power": 10
        }],
        "sleep": [{
            "id": 0,
            "name": "s0",
            "power": 5,
            "latency": 1
        }]
    }
}
```

Fig. 2. CPU core model description

With this approach multiple CPU cores, each having its own power state model, can be instantiated and multiprocessor systems can be simulated.

B. Program load model

Program load consists of tasks. Tasks are simulation objects which have priority as parameter. Priorities from 0 to 63 are supported, where 0 is the highest and 63 the lowest priority. Tasks are modeled as number of single clock instructions that CPU core executes.

After tasks are initialized, they are ready to execute (Fig. 3). If multiple tasks are ready, then task with highest priority becomes active. Tasks can be pre-empted by tasks with higher priority. Tasks can also become blocked while waiting on a synchronization element to become available. After synchronization element becomes available, tasks waiting on it become ready to execute.

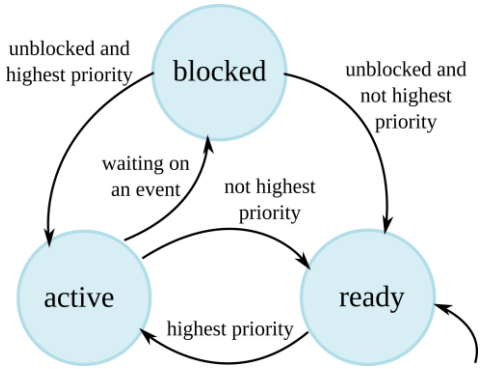

Fig. 3. Task state machine

IV. RESULTS

Functionalities of the simulation system example are verified using two different optimization algorithms. First algorithm is single processor Dynamic Frequency scaling, which is a power management algorithm. Second algorithm is Multiprocessor Load Balancing.

A. Single processor DFS

DFS algorithm presented in [11] has been implemented in simulator. Single CPU core is used with power states presented in Table 1. Two types of tasks are executing on the CPU core, time-critical task (Task #1 in Fig. 4) and non-critical task (Task #2 in Fig. 4). DFS algorithm (simulation manager) is implemented as two tasks, the DFSHP and DFSLP task. DFSHP task is used to capture timestamps of start and end of execution of time-critical task. DFSLP task is used to calculate CPU utilization of time-critical task execution and calculate next frequency that is to be configured in order to reduce power consumption. Programming model and task synchronization is presented in Fig 4.

TABLE 1
PROCESSOR STATES DESCRIPTION

CPU active states			CPU inactive states		
State	**Power [mW]**	**Freq [MHz]**	**State**	**Power [mW]**	**Latency [us]**
A0	160	8	**idle**	10	N/A
A1	119	6	**S0**	1	1
A2	75	4	**S1**	0.1	10
A3	43	2			

For configured time-critical task workload of 22000 instructions and incoming event every 16ms, task execution diagram is presented in Fig 5. With this configuration, DFS algorithm provides 9% power savings.

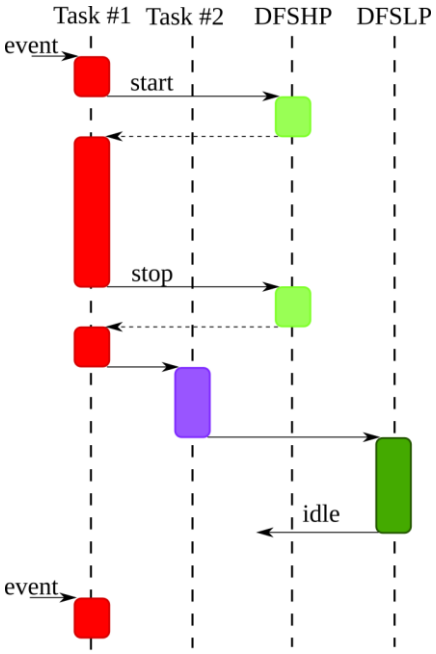

Fig. 4. Programming model and task synchronization for single processor DFS example

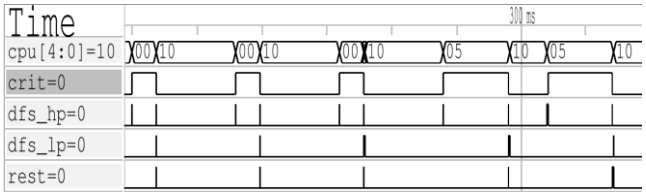

Fig. 5. Task execution diagram for DFS

B. Multiprocessor load balancing

Typical multiprocessor embedded system can have several processor cores each with different power model and working at different clock frequency. Critical processing is usually distributed among these processor cores in a form of parallel programming threads. Although

simulator can support different system architectures, presented results consider centralized architecture with multiple CPUs each executing one thread of a critical programming task and central, manager CPU dedicated for results aggregation and system control. Programming model and task synchronization is depicted in Fig 6.

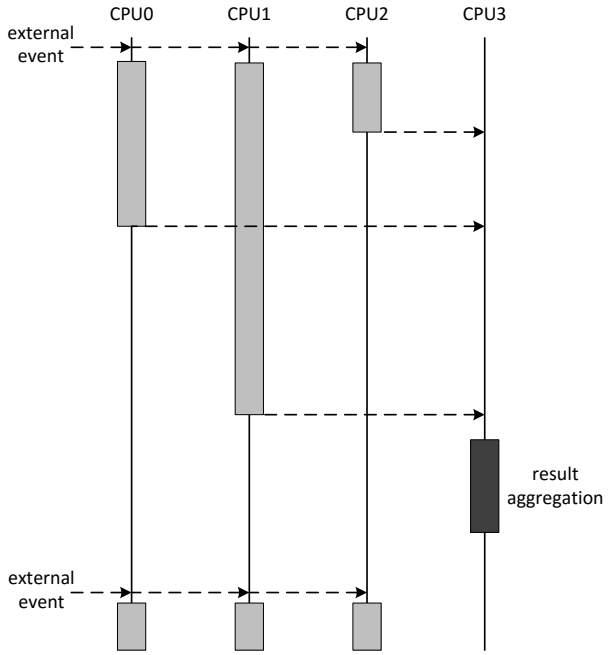

Fig. 6. Programming model and task synchronization for typical centralized multiprocessor embedded system

In the presented simulation scenario start of processing on all cores in the system is triggered by external event which is generated periodically inside simulation environment. Manager CPU waits while all other CPUs in the system finish their processing to aggregate results and provide final output. Since tasks executing on different cores can have very different complexities in terms of instruction count, and since each core can work at different frequency, load of different cores in the system can vary very much. This particularly means that some cores will spend majority of the time in Idle or Low power state. Although this can be beneficial in terms of total energy consumption, peak power that they exhibit can be very high. Load balancing is a process of equalizing utilization of all working cores in the system. Balancing the load of multiple processors will minimize this peak power while ensuring that all timing deadlines are met. Architecture of embedded multiprocessor system with property of dynamic load balancing is shown in Figure 7. Cores CPU0, CPU1 and CPU2 are worker cores while CPU3 is manager core responsible for result aggregation and power optimization of the entire system. Each core measures its own utilization in the same manner as explained previously in the DFS example. Statistics about utilization along with processor's unique ID are written into *statistics* shared memory.

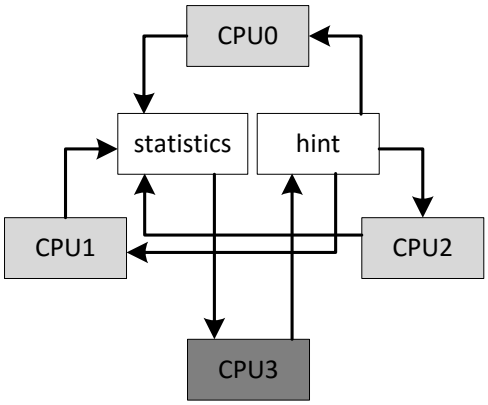

Fig. 7. Architecture of multiprocessor system with 3 worker and 1 manager core, with ability of load balancing

Manager core CPU3 waits until all worker cores update their statistics to execute optimization algorithm. Output of the optimization algorithm could be the set of recommended working frequencies for each worker core in the system. However, there are no guarantees that this particular optimum can be achieved since all cores have different discrete set of available active states and different working frequencies. Also, changing utilization of one CPU core can influence utilization of other CPU cores if programming threads which are executing on them are interdependent. On the other hand, iterative step by step optimization assumes that at the each optimization period manager core will send just one optimization hint to the worker core with the least optimal utilization whether it should increase or decrease its working frequency. Upon receiving this hint worker core initiates transition to the next closest state with larger or lower working frequency depending on the actual hint value, as it is shown in Fig. 8.

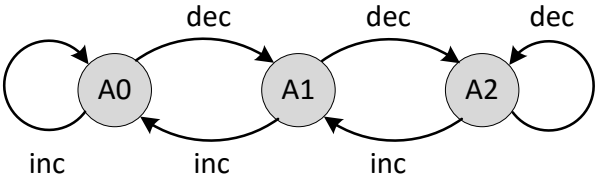

Fig. 8. State transitions triggered by the optimization hint

When one processor changes its state, utilization of other processors in the system can also change because of dependencies between them. At the next optimization step manager will calculate new hint value which will be based on this newly established system utilization and thus will move the whole system step by step to the optimal working mode.

Simulator is tested with two different scenarios of load balancing of heterogeneous multiprocessor system with 2 worker and 1 manager core.

In the first scenario each worker core is executing same amount of instructions. However, they have different

starting frequencies and different set of available active power states as it is shown in Table 2. Because of this, initial utilizations of these two worker cores will be very different as it is shown in Fig. 9. a).

TABLE 2
PROCESSOR STATES DESCRIPTION

CPU0 active states			CPU1 active states		
State	**Freq [MHz]**	**Power [mW]**	**State**	**Freq [MHz]**	**Power [mW]**
A0	20	200	**A0**	5	120
A1	8	80	**A1**	2	48
A2	5	50	**A2**	1	21
A3	2	20			
A4	1	10			

Manager core detects this load imbalance and sends a hint to CPU0 to decrease its working frequency resulting in transition from state A0 to the state A1, Fig. 9. b). At the next optimization period manager core detects that CPU0 still has much lower utilization than CPU1 and sends another hint for lowering working frequency resulting in transition to the state A2, Fig. 9. c). Since in the state A2 processor CPU1 has the same working frequency as CPU0 and since they are executing same programming load their utilization will be equal.

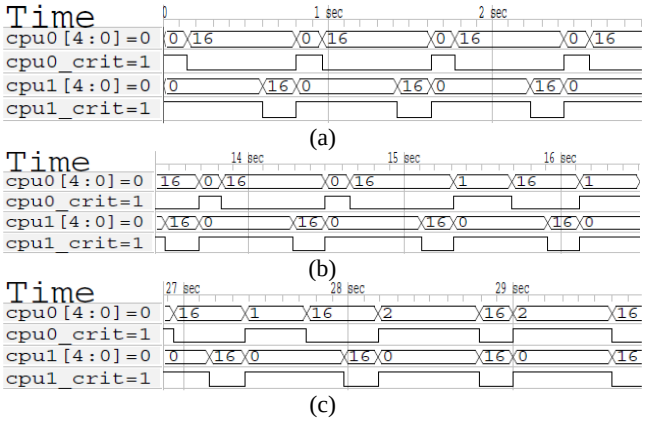

Fig. 9. Load balancing process of different worker cores executing same programming load

In the second scenario two same worker cores with the set of active power states shown in Table 3, are executing different amount of programming load. Programming thread executing on CPU0 has 3000 instructions while programming thread executing on CPU1 has 1300 instructions. This will cause unequal utilization of these two worker cores. CPU1 will have much lower utilization than CPU0, Fig. 10. a).

TABLE 3
PROCESSOR STATES DESCRIPTION

CPU active states		
State	**Freq [MHz]**	**Power [mW]**
A0	5	120
A1	2	48
A2	1	21

Manager core detects this load imbalance and sends a hint to CPU1 to decrease its working frequency, resulting in transition from state A0 to the state A1, Fig. 10. b). After this transition utilization of these cores are almost equal. Since small imbalance in utilization is tolerated by the manager core, no further hints will be sent for performance adjustment.

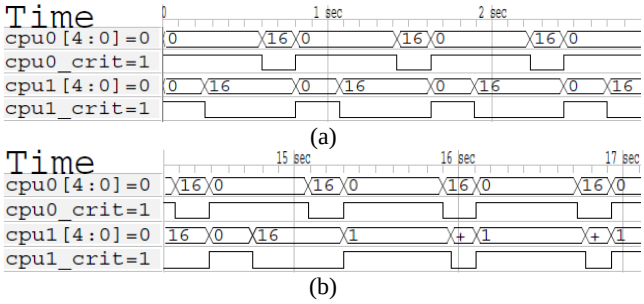

Fig. 10. Load balancing process of worker cores with same characteristics executing different amount of programming load

V. Discussion

Energy-aware embedded system simulator is presented. Example implementation is provided based on presented concept and its functionality has been verified using two algorithms with different optimization goals, power management and load balancing.

Compared to already existing simulators, presented concept provides simple interface and allows easy system model description, while taking into account power consumption of the system. Presented concept can be used to develop and evaluate scheduling, and power and performance management algorithms for single processor and multiprocessor embedded systems. Simulation model can be further extended to incorporate more complex entities and to provide means to accurately estimate system power consumption.

ACKNOWLEDGEMENT

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The Power Quality Estimation by Integrated Power Meter DSP Block

Borisav Jovanović, Predrag Petković, Milunka Damnjanović

Abstract - The paper considers the main features of the digital signal processing block which is embedded in a three-phase integrated power meter IC. The DSP block adds new features to modern power metering units including power quality measurement. The operations that DSP performs, are described thoroughly in the paper.

Keywords - Digital signal processing.

I. Introduction

Recent integrated circuit (IC) fabrication technologies enabled design of complex systems on the same chip area, greater clock frequencies and less dynamic component of power consumption. A representative of such complex electronic system is an integrated power meter, which digital signal processing (DSP) block is proposed in the paper. The DSP is dedicated for utilization in power metering systems. The paper explains the most significant DSP's features, which enables its integration in modern smart power meters.

Present power metering units rarely provide power quality information. Although there are several commercially available ICs dedicated to power metering applications, none of these solutions provides all necessary power quality information, important in the electrical grid systems with nonlinear loads. Present power metering units are not able to detect and quantify the distortion level at consumer site. Instead, expensive methods and devices are used, usually at higher levels of electrical energy distribution.

Previous versions of designed DSP block [1] were dedicated principally to metering of power consumption. The chip has ability to calculate root mean square values of voltage and current, active, reactive, apparent power and energy. In addition to results related to power consumption and energy, novel DSP provides several power quality measures. To quantify power quality, DSP calculates distortion power (D) and total harmonic distortion (THD) Moreover, the presence of voltage signal sags can be detected. Incorporated in power metering unit, the power signal quality is determined at sites where consumers access the electrical grid.

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II. The digital signal processing (DSP) block

A. The DSP's main features

DSP is a part of Integrated power meter chip which contains also Sigma-delta AD converters [2], digital filters and an 8051 microcontroller. At inputs, the DSP gets digital samples from the other blocks - the Sinc and FIR digital filters (Fig.1). The input signals consist of current I, voltage V and phase shifted voltage V_P for all three power grid phases. Besides them, DSP gets the digital samples of instantaneous neutral line current value and chip temperature gets. The sampling frequency of these signals is 4000 samples per second, and signal resolution is 18 bits. The DSP operates at clock frequency equal to 8.192 MHz.

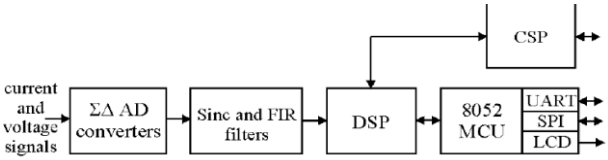

Fig. 1. The DSP block as a part of Integrated power meter

The DSP periodically, once in one second time interval, calculates following parameters:

- root mean square values of current I_{RMS} and voltage V_{RMS} for all three phases,
- root mean square value of neutral line current I_{NULL},
- the chip temperature T,
- average active P_{AV}, reactive Q_{AV}, distortion D and apparent S power in all three phases,
- power factor $Cos(\varphi)$,
- the voltage signal frequency f_{LINE},
- the values of 1., 3., 5. and 7. harmonic of current signal in all three phases,
- the current signal THD values,
- values of first harmonic of voltage signal in all three phases,
- voltage signal THD factor.

The input dynamic range for current is from 10mA to 100A and for voltage is up to 300V. The results are obtained for all three electrical grid phases.

B. The main architecture of DSP

The DSP architecture can be divided into data path and

control unit. The data path is comprised of five smaller sub blocks, denoted with Block 1 to Block 5, and additional serial communication block.

Block 1 performs arithmetically intensive calculations, including the accumulation of instantaneous samples of I^2, V^2, P and Q. The sums are needed for calculation of I_{RMS}, V_{RMS}, P_{AV} and Q_{AV}. The Block 1 measures the active, reactive and apparent energy. The Block 1 operations will be further described in detail.

Block 2 is used for calculation of: root mean square values V_{RMS} and I_{RMS}, the power factor $Cos(\varphi)$, the active P_{AV}, reactive Q_{AV}, distortion D and apparent power S, chip temperature T, the voltage signal frequency f_{LINE}, the first harmonic for voltage signal, the 1., 3., 5. and 7. harmonic for of current signal.

Block 3 calculates intermediate results that are needed for calculation of current and voltage harmonics and later, corresponding THD factors. Block 2 uses these intermediate results during its calculation process.

Block 4 is 512x24 bits RAM memory block. The RAM is used for storing the calibration data, final and intermediate results that DSP calculates.

Block 5 is a control unit. It is implemented as finite state machine, periodically performing the state sequence lasting 2048 clock cycles. The state sequence is repeated 4000 times during one-second time interval. The state sequence can be divided into four equal intervals consisting of 512 clock cycles denoted as R, S, T and E.

The DSP block results are available to external microprocessor systems (Baseband processor) through serial communication interface. The Baseband processor is able to loads the DSP's calibration registers or to read the measurement results. This feature adds flexibility to the proposed system, which causes that the DSP can be easily embedded in many power grid-metering devices.

C. DSP's control unit operation

The control unit is comprised of four smaller control units; three of them are physically implemented in blocks 1, 2 and 3. The units control the following operations:

- data transfer inside the data path blocks,
- data path transfer at block's interface,
- arithmetical calculations.

The Fig. 2 presents main control unit intervals. During intervals R, S and T, Block 1 calculates instantaneous values of I^2 voltage V^2, active P and reactive power Q. These operations are identical for different phases, except the data is stored at different locations of RAM memory. During R, S and T, Block 3 calculates intermediate results, which are further used for current and voltage signal harmonics and THD factors.

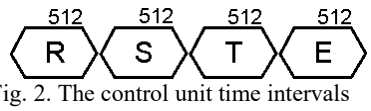

Fig. 2. The control unit time intervals

During interval E, Block 2 calculates final results - V_{RMS}, I_{RMS}, $Cos(\varphi)$, P_{AV}, Q_{AV}, S, D, chip temperature, frequency, harmonics and THD values. After chip is reset, E subsequence is also used for DSP's initialization (loading the DC offset and gain calibration registers for current and voltage signals).

D. The arithmetical operations performed by Block 1

Control unit 1 performs identical sequences in phases R, S and T. The operations are executed 4000 times per second. At the beginning of sequence, DC offset is suppressed in current, voltage and phase-shifted voltage signals. The DC offset can be rejected by High pass filter (HPF) or after DC offset is subtracted from instantaneous current and voltage values (Fig. 3). An Infinite Impulse Filter (IIR) which cut-off frequency is set to 5Hz implements the High pass filter. The transfer function of High pass filter is:

$$H_{HPF}(z) = (1-2^{-10})\frac{(1-z^{-1})}{1-z^{-1}(1-2^{-9})} \tag{1}$$

The Eq. (1) is transformed into Eq. (2), where filter register are expressed in form of RAM memory registers:

$$Ifilt = Ifilt(1-\frac{1}{2^9}) + (2^{10}-1)(I1-I3) \tag{2}$$

$$I2 = Ifilt/1024 \tag{3}$$

In Eq. (2) and (3) I_1 and I_3 are two consecutive current samples, I_{filt} is the 48-bit HPF filter register, which content is equal to current AC component, multiplied with 1024. The signal I_2 in Eq. (3) is AC component of current signal. Arithmetical units within Block 1 perform all arithmetical operation (addition, subtraction and shifting). The identical sequence of operation is executed for voltage DC offset discrimination (Fig.3).

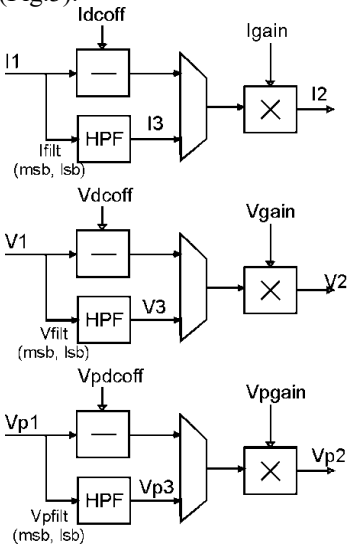

Fig. 3. The operations for DC offset eliminations

The AC component of current signal I_2 is first squared. Then, the squared result is passed through Low-pass filter.

The result is accumulated in the register AccI2.

The LPF is implemented as an IIR filter and has main goal to reduce I_{RMS} calculation error. Namely, LPF decreases AC component of square of instantaneous current signal. The chosen cut-off frequency is 10Hz. The filter's transfer function is:

$$H_{LPF}(z) = \frac{2^{-6}}{1 - z^{-1}(1 - 2^{-6})} \quad (4)$$

The transfer function can be rearranged to:

$$I2filt = I2filt(1 - \frac{1}{2^6}) + I2xI2 \quad (5)$$

$$(I2xI2)_{DC} = Ifilt / 64 \quad (6)$$

where I_2 is an AC component of instantaneous current and *I2xI2* is its squared value. The *I2filt* is 48-bit IIR filter register. The DC component is obtained after dividing the number I2filt by constant 64. At the end, the result is added to AccI2 (Fig. 4). Similar operations are performed by Block 1 for voltage signal processing. The following registers are used: 24-bit V2, 48-bit HPF register V2filt and 48-bit register AccV2. The active and reactive instantaneous power are processed similarly (presented in Fig. 4).

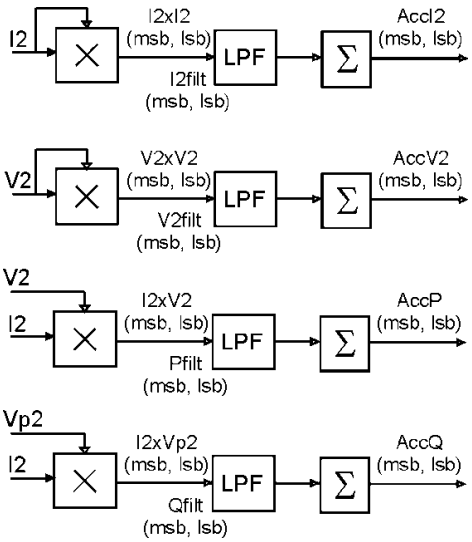

Fig. 4. The operations for multiplication, filtering and accumulation of AC components of current, voltage and phase shifted voltage signals.

E. The arithmetical operations performed by Block 2

During E subsequence (Fig. 2) operators in Block 2 calculate final results - V_{RMS}, I_{RMS}, $Cos(\varphi)$, P_{AV}, Q_{AV}, S and D. Based on AccI2, I_{RMS} is derived as the result of following operations. First, AccI2 is divided by number 4000 - the number of accumulation operations in I_{RMS} calculation period. Then, the AC offset (I2off in Fig.5) is subtracted (shown in Fig.6). I_{RMS} is obtained after square root operation is performed.

The same hardware is used for V_{RMS} calculation. At start of operation, the AccV2 is used. For offset correction the register V2off is used. The final result is stored in register V_{RMS}.

The similar method is used for calculation of P_{AV} and Q_{AV}. The difference is that there is not square root operation (Fig.5).

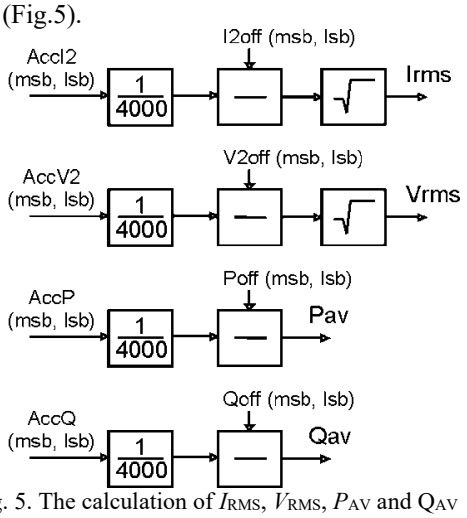

Fig. 5. The calculation of I_{RMS}, V_{RMS}, P_{AV} and Q_{AV}

The apparent power S is obtained when I_{RMS} and V_{RMS} are multiplied. After that, average active power P_{AV}, reactive power Q_{AV} and apparent power S are used for calculation of distortion power D [3], [4]. The operation sequence is given in the Fig. 6.

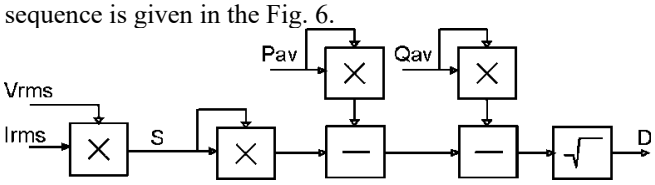

Fig. 6. The calculation of apparent power S and distortion D

F. The active, reactive and apparent energy measurement

New results for P_{AV}, Q_{AV} and S are obtained every second and they are used for measurement of active, reactive and apparent energy. The DSP block has six pins for the energy results. The pins are named with Pulse 1 to Pulse 6. The pulses are programmed in DSP's control registers:

- if pin produces the pulses for some particular phase or all three phases,
- if pin produces pulses for active, reactive or apparent power
- if positive or negative energy is measured
- the pulse width can be changed in range from 10 to 40 ms

To generate pulses for measured active energy, P_{AV} is accumulated in 48-bit register AccEa (the part of RAM memory). After the addition operation is performed, the AccEa is compared to referent energy value (stored in register Energy_P). If AccEa is greater than Energu_P, a

pulse is on output pin is generated. If active power value P_{AV} is negative (in case when electricity generators are measured), when the negative sum AccEa is obtained, a pulse for negative energy is generated and Energy_P is added to AccEa. The hexadecimal value Energy_P=0x1E000000 gives the proportion of 1000 pulses for energy of 1kWhr. This proportion can be changed in the range from 100 to 100000 pulses per 1kWhr.

The similar operations are executed for reactive energy measurement. The registers Q_{AV}, Energy_Q and AccEq are used. The Energy_ Q defines the number of pulses per 1kVaR.

G. Power quality - the harmonics and THD calculation

The Goerzel algorithm [5] has been implemented for calculation of 1., 3., 5. and 7. harmonics for the current signal. Additionally, the DSP provides that harmonic order can be changed. The order is specified by a DSP control register.

The circuit gets at inputs current and voltage samples, at 4000Hz sampling frequency. The Goertzel algorithm consists of two parts: the iterative and final part. The iterative part is executed 4000 times per second. In final algorithm step, the real and imaginary parts of complex spectral component are found. The iterative part of algorithm is executed by Block 3, while the final part is done within Block 2.

The method for obtaining the k. harmonic is described as follows. In the method, as auxiliary registers, the 48- bit Q_0, Q_1 and Q_2 are used. At the beginning of iterative operation, Q_0, Q_1 and Q_2 are reset. Next, in every iteration step, for each input sample, new values of Q_0, Q_1 and Q_2 are derived [5] according to:

$$\begin{aligned} Q_0 &= 2 \cdot Q_1 \cdot \cos(2\pi \cdot \frac{50 \cdot k}{4000}) - Q_2 + X_{IN}; \\ Q_2 &= Q_1; \\ Q_1 &= Q_0 \end{aligned} \tag{7}$$

At the end of iterative algorithm part, the real and imaginary parts of a complex number are:

$$\begin{aligned} real &= \frac{1}{2000}\left(Q_1 - Q_2 \cdot \cos(2\pi \cdot \frac{50 \cdot k}{4000})\right) \\ imag &= \frac{Q_2 \cdot}{2000} \cdot \sin(2\pi \cdot \frac{50 \cdot k}{4000}) \end{aligned} \tag{8}$$

The k. harmonic is found as:

$$y^k = \sqrt{real^2 + imag^2} \tag{9}$$

The harmonics are stored in 24-bit registers. The circuit calculates the THD factor [5]:

$$THD = \frac{1}{I_{1,RMS}} \sqrt{I_{RMS}{}^2 - I_{1,RMS}{}^2} \tag{10}$$

H. Implementation results

The DSP block is successfully verified after extensive simulations are performed. The parts of a DSP circuit, which calculates the electrical power system parameters, are particularly verified. The circuit has been implemented in technology AMI 180nm and occupies 0.5mm^2 area.

III. Conclusion

Many different power metering functions are implemented in the same chip. DSP achieves high performances at the levels as those obtained with commercial DSP microprocessors and consumes less power consumption. Since it calculates harmonics, THD and distortion power, the DSP can be easily embedded in devices dedicated to power quality measurement, especially when nonlinear loads are present in the grid.

Acknowledgement

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Monitoring and Compensation of Harmonics in Smart Grid

Dejan Stevanović, Marko Dimitrijević, Miona Andrejević Stošović, and Predrag Petković

Abstract - In this paper we will try to present the current state concerning monitoring and compensation of harmonics in smart grid. We will discuss the existing harmonic detection techniques, and present harmonic reduction techniques that are usually used. We will give some measured results that will show that existing techniques are not good enough, suggesting that new techniques should be proposed.

Keywords -Compensation, Filters, Harmonics, Monitoring, Smart Grid.

I. Introduction

Nowadays, when electronic devices became ubiquitous, we are witnessing changes in the demand and energy use. It is presumed that the overall household consumption for electronic appliances will rise with a rate of 6% per year so reaching 29% of the total household consumption in the year 2030. In the same time, the household consumption is expected to reach 40% of the overall electricity demand. The immense rise of the office consumption due to the enormous number of computers in use is also to be added. That stands for educational, administrative, health, transport, and other public services, too. One may get the picture if one multiplies the average consumption of a desktop computer (about 120 W) with the average number of hours per day when the computer is on (about 7), and the number of computers (billion(s)?)[1].

Also, efficiency of electrical distribution is rarely planned or managed by utilities. The unfortunate result is that most utilities waste substantial amounts of electricity. In fact, annual electricity transmission and distribution losses average 6% in the European Union (assuming that 2% is for transmission and 4% is for distribution losses) [2]. That represents 7 billion Euros in energy wasted every year in distribution. This number includes losses in the medium and low voltage lines and in primary and secondary substations. Many countries have brought the law that demands from utility to reduce the losses for 1.5% each year [2].

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Understanding grid losses, their origin and determination, is important considering energy efficiency and grid regulation. These losses can be classified as *technical losses* and *non-technical losses.*

Technical losses are the result of the inherent resistance of electrical conductors, which causes electrical energy to be transformed to heat and noise whenever current flows through them. This is usually referred to as 'physical (or ohmic) losses'. Technical losses vary with the level of utilization of the network capacity, i.e. the quantity of electricity being transmitted/distributed. In particular, they are proportional to the square of the current. As a result, transmission networks experience a lower level of losses because at higher voltages a lower current is required to transmit the same amount of electric energy. Conversely, distribution networks (at lower voltages) are subject to a higher level of losses.

On the other hand, non-technical losses comprise electricity that is delivered mostly for consumption but which is not paid for. They are mainly caused by in-house consumption (also known as "hidden" losses); the illegal abstraction of electricity (energy theft); non-metered supplies (such as public lighting); as well as errors in metering, billing and data processing. Additionally, there are errors resulting from the time-lag between meter readings and statistical calculations. According to Schneider Electric about 90% of non-technical losses occur in the medium and low voltage (MV/LV) grid. It is assumed that they range between 1.000€ to 10.000€ per MV/LV substation per year in European countries [2]. This brought MV/LV grid at the top of the priorities for loss reduction.

In order to reduce the level of losses at a power grid, many different approaches exist, some of which are published in [2]. In this paper, we will consider non-technical losses.

The first step in cutting the losses is to monitor and to detect their sources. This request was hardly feasible and very expensive in the past. Fortunately, that is not the case today. Smart meters give inexpensive and precise insight into the current status of particular parameters of the grid. They allow the utility to measure many parameters that define quality of the delivered electric power. Unfortunately, due to the inertia of the acceptance of facts, some decisions affecting the power system are not timely made.

The most obvious misconception is related to

understanding the character of consumers connected to the electricity grid. The standpoint of the power grid measurement theory assumes that all loads are entirely linear resistive or reactive. This implies that the current follows voltage sine waveform (with possible phase lead or lag at reactive loads). In general, for centuries the loads in households were basically resistive (heaters, incandescent light) while in industry they usually have large inductive character (AC motors). Consequently, it was sufficient that power meters register only active power in households and/or reactive power with industrial customers. However, the character of loads has been drastically changed since the last quarter of the 20th century. Namely, electronic loads nowadays are strongly related to the power quality thanks to the implementation of AC/DC converters that in general draw current from the grid in bursts. The current-voltage relationship of these loads, looking from the grid side, is nonlinear, hence nonlinear loads. In fact, while keeping the voltage waveform almost sinusoidal, they impregnate pulses into the current so chopping it into seemingly arbitrary waveform and, consequently, producing harmonic distortions. Having all this in mind the means for characterization of the load from the nonlinearity point of view becomes one of the inevitable tools of quality evaluation of smart grid.

Due to the nonlinearities, measurement of power factor and distortion, however, usually requires dedicated equipment. For example, use of a classical ammeter will return incorrect results when attempting to measure the AC current drawn by a non-linear load and then calculate the power factor. A true RMS multi-meter must be used to measure the actual RMS currents and voltages and apparent power. To measure the real power or reactive power, a wattmeter designed to properly work with non-sinusoidal currents must be also used.

In this paper, we will first give some existing solutions (...), and after that we will propose how to upgrade the meters and billing policy in order to reduce economic losses at utility [3]. We will also propose a measurement system in order to establish a comprehensive picture about the properties of a given load, i.e. to perform complete analysis of the current and voltage waveforms at its terminals. In that way the basic and the higher harmonics of both the current and the voltage may be found.

II. HARMONIC DETECTION AND MEASUREMENT

In linear circuits, consisting of linear loads, the currents and voltages are sinusoidal and the power factor effect arises only from the difference in phase between the current and voltage. When nonlinear loads are present one should introduce new quantities in the calculations emanated by the harmonics and related power components. Now the power factor can be generalized to a total or true power factor where the apparent power, involved in its calculations, includes all harmonic components. This is of importance in characterization and design of practical power systems which contain non-linear loads such as rectifiers, and especially, switched-mode power supplies. Phase difference between current and voltage, as well as harmonic distortion has negative impact on distribution system.

Since the problem of distortion becomes ubiquitous, it can be either observed at the distribution system level, or one has to take local measurement of the properties of this kind of loads.

Measurement of power factor and distortion, however, usually requires dedicated equipment. For example, use of a classical ammeter will return incorrect results when attempting to measure the AC current drawn by a non-linear load and then calculate the power factor. A true RMS multimeter must be used to measure the actual RMS currents and voltages and apparent power. To measure the real power or reactive power, a wattmeter designed to properly work with non-sinusoidal currents must be also used.

In recent papers [4], a new approach to polyphase load analysis is presented: system for nonlinear load characterization which is flexible, scalable, with advanced options.

This solution brings all benefits of virtual instrumentation, keeping main advantage of classical instrument – determinism in measurement. The hardware component of the system is implemented using field programming gate array (FPGA) in control of data acquisition. The software part is implemented in two stages, executing on real-time operating system and general purpose operating system. Described realization provides possibility for calculating a large number of parameters that characterize nonlinear loads, which is impossible using classical instruments. This is of great importance particularly in calculation of alternate definitions of reactive power. The system is scalable; it can be upgraded in number of calculated parameters, as well as in number of independent measurement channels or functionality. The system is open; it can be modified to be a part of harmonic compensation circuitry or aimed for hardware-in-the-loop simulations. The system is flexible; it is implemented on different platforms for different purposes: as laboratory equipment for real time measurements (PXI controller equipped with PXI-7813R FPGA card and expansion chassis), as compact industrial device for real time operation (installed on programmable automation controller) or simple portable instrument equipped with computer interface. It consists of three subsystems: acquisition subsystem, real time application for parameter calculations and virtual instrument for additional analysis and data manipulation.

Acquisition subsystem consists of acquisition modules for A/D conversion, FPGA circuit and interface for computer or programmable automation controller. A/D resolution is 24-bit, with 50 kSa/s sampling rate and dynamic range ±300 V for voltages and ±5 A for currents. Function of FPGA circuit is acquisition control and

harmonic analysis.

Real time application calculates power and power quality parameters deterministically and save calculated values on local storage. The application is executed on real time operating system.

Virtual instrument for additional analysis and data manipulation represents user interface of described system. It runs on general purpose operating system, physically apart from rest of the system. Communication is achieved by TCP/IP. Parameters and values obtained by means of acquisition and calculations are presented numerically and graphically.

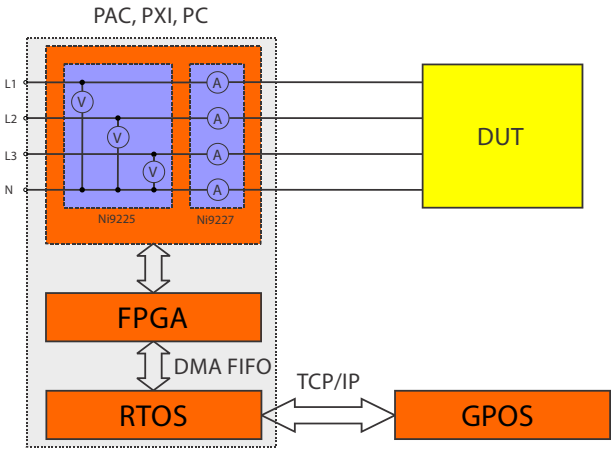

Fig. 1 System architecture

III. HARMONIC REDUCTION TECHNIQUES

The permanent growth of the number and types of nonlinear loads aggravates the problems caused by harmonics. That enforced almost every country to introduce its own standard that restricts the allowed amount of each harmonic. Two widely known standards in this area are the IEEE 519-1992 and IEC 61000 series. The both standards regulate limits for the harmonics pollution but do not specify what happens if a customer exceeds them. There are two possibilities: the first suggests that the utility could disconnect that customer, but that is stressful and not profitable solution. The better way and the most effective tactic is to charge the harmonics producers a penalty tax if they exceed limits of harmonics pollution. The penalty tax should be proportional to the pollution levels. However, the tax driven regulation may be obstructed by two technical problems: the identification of the harmonics producers, and isolation of the system from the effects of impedance variation.

The harmonic mitigation at power system can be solved in two ways that can be divided to preventive and corrective. The preventive solution includes: phase cancellation or harmonic control in power converter and developing procedure and methods to control, reduce or eliminate harmonic in power system equipment; mainly capacitor, transformers and generators.

If harmonic isn't eliminated at load's level, then some of corrective techniques must be used to reduce existing harmonics at power grid. The corrective techniques are based on few different types of harmonic filters. Traditionally, passive filters have been used but some problems are associated with them. A passive filter consists of a series circuit of reactors and capacitors. Harmonic currents generated by, for example, a frequency converter are shunted by this circuit designed to have low impedance at a given frequency compared to the rest of the network. Figure 2 illustrates schematically the described function with a harmonic generator, impedance representing all other loads, a filter and a network.

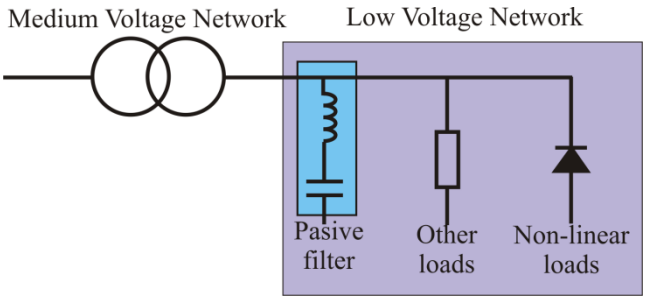

Figure 2. Passive filtering of harmonic

As the passive filters offer very low impedance at the resonance frequency, the corresponding harmonic current will flow in the circuit whatever its magnitude. Passive filters are then easily overloadable under which condition they will switch off or be damaged. The overload may be caused by the presence of unforeseen harmonics on the supply system or be caused by structural modifications in the plant itself (such as the installation of a new drive). Passive filter provides always a certain amount of reactive power. This is not desirable when the loads to be compensated are AC drives which have already a good power factor. In that case the risk of overcompensation exists as a result of which the utility may impose a fine.

The degree of filtering of the passive filter is given by its impedance in relation to all other impedances in the network. As a result, the filtration level of a passive filter cannot be controlled and its tuning frequency may change in time due to ageing of the components or network modifications. The quality of the filtration will then reduce. It is also important to note that a passive filter circuit may only filter one harmonic component, so a separate filter circuit is required for each harmonic that needs to be filtered.

Fortunately the number of manufacturers being aware of the problems caused by their product increases. So, they try to improve their product using different filtering methods in order to reduce value of generated harmonics. For example, most of Phillips branded LED use the Valley-fill circuit [5, 6]; Toshiba lamp contains a passive filter [7, 8], while Osram decides to embed an active filter [7, 8].

Despite the used filter the current of these loads is not sinusoidal [7]. In order to overcome the problems associated with traditional passive filters and in order to answer to the continuing demand for a good power quality, active filters for low voltage applications are developed.

The principle of active filtering is fundamentally different from that of the passive filter. It was noted previously that the passive filter is not controlled and that the filtering is a result of the impedance characteristics. The active filter instead measures the harmonic currents and generates actively a harmonic current spectrum in opposite phase to the distorting harmonic current that was measured. The original harmonics are thereby cancelled. The principle is shown in Figure 3.

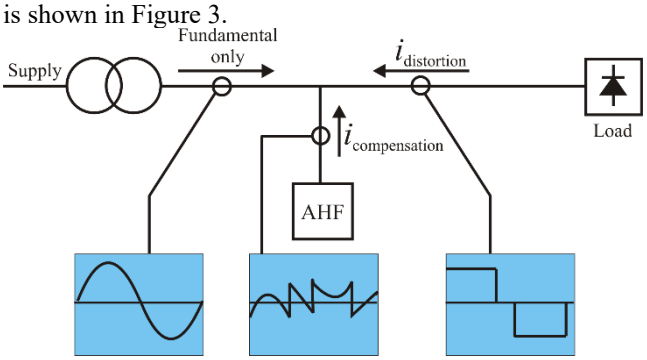

Figure 3. Principle of active filtering

The control of the active filter in combination with the active generation of the compensating current allows for a concept that may not be overloaded. Harmonic currents exceeding the capacity of the active filter will remain on the network, but the filter will operate and eliminate all harmonic currents up to its capacity. It can also be noted that the active filter we are considering here has a parallel topology. Active filters also exist in series topology but they do not offer the same advantage as the parallel topology: the connection is much less flexible; it has higher losses and is overloadable like the passive filter. From this point onwards, "active filter" will only refer to the parallel topology. The principle of active filter showing currents and spectra is clarified in Figure 4.

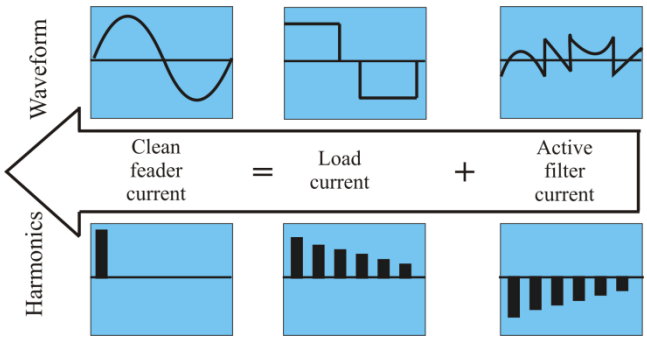

Figure 4. Active filter principle illustrated in the time and frequency domain

IV. Measurement Results

As we said in previous section many manufacturers of nonlinear loads are aware of problems that are caused using their product. So they start with implementing different filters inside their gadget. By implementing these filters the level of harmonics is reduced, but they are not eliminated. Therefore, we will here show the current waveform for different type of CFL and LED bulb. These waveforms are obtained by using measurement equipment described in section II. Figure 5 presents current waveform of different CFLs manufactured by General Electric.

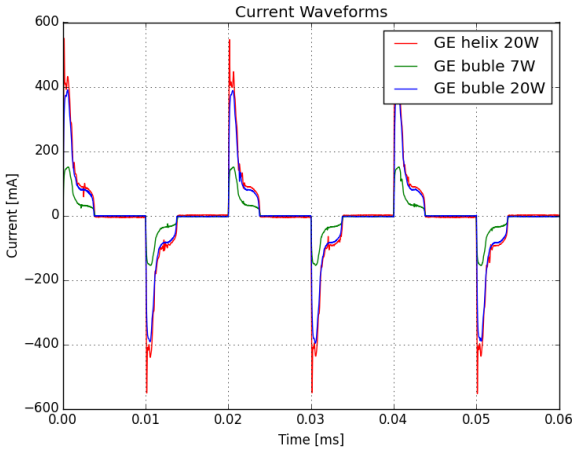

Figure 5. Current waveforms of different types of CFL

From Figure 5, it is clear that the current waveforms of different wattage lamps have the same shape, although the magnitude of current increases with the increase of power rating. In the Figure 6 we presented the current waveforms obtained from different LED lamps. This figure indicates that dissimilar LED bulbs use different filtering methods to reduce harmonic generation. Some of these methods are more efficient than others.

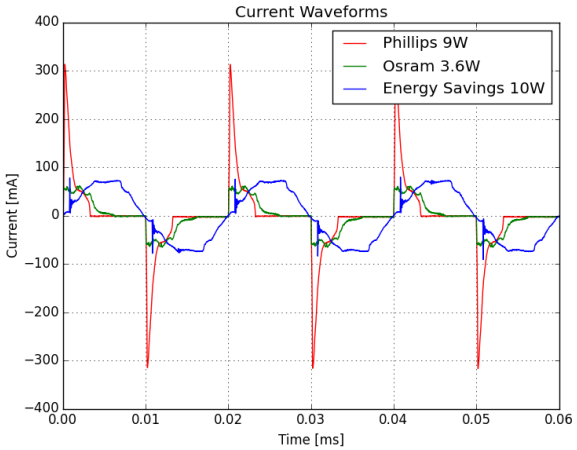

Figure 6. Current waveforms of different types of LED bulb

The Figure 5 and 6 clearly show that harmonics still exist, despite the filters that are implemented to reduce

them. Consequently, loads with these filters still produce the considerable value of harmonics and some improvement of these filters is necessary. However, the question is whether it can be paid off to the manufacturer. An alternative is to employ some active harmonic compensation systems at PCC [9]. Therefore, harmonics produced by all nonlinear loads connected at PCC will be diminished and manufactures cost will be less. However this opens a new topic - who should to pay for this system: customer or utility.

V. Conclusion

In this paper we discussed the existing harmonic detection and harmonic reduction techniques that are usually used. Principles of passive and active filtering are explained. Measured results are given for different types of LED and CFL bulbs, showing that despite the filters that are implemented to reduce them, harmonics still exist. The conclusion is that some more efficient techniques must be proposed.

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One-Week- and One-Month-Ahead Prediction of Suburban Electricity Load

Jelena Milojković, Slobodan Bojanić, Octavio Nieto, and Vančo Litovski

Abstract - It will be shown here first time that for the subject of short term prediction of electricity load, even though a large amount of data may be available, only the most recent of it may be of importance. That gives rise to prediction based on limited amount of data. Then, we propose implementation of some instances of architectures of artificial neural networks as potential systematic solution of that problem as opposed to heuristics and statistical ones that are in use. Since prediction when implemented in a real time system has no reference to be valuated, two independent mutually supporting predictions of the same quantity will be generated the results being averaged to produce the final one. A specific approach to the evaluation of the number of hidden neurons will be implemented. All these lead to a completely new procedure for one-step-ahead prediction of electricity loads at suburban level. Examples will be given related to monthly and weekly forecasting of the electricity load. Prediction is carried out on real data taken from the literature. Small prediction errors were experienced.

Keywords— forecast, load prediction, electricity, artificial neural networks

I. Introduction

Electric load prediction is essential for power generation and operation [1]. It is vital in many aspects such as providing price effective generation, system security, and planning. Among others, it enables: scheduling fuel purchases, scheduling power generation, planning of energy transactions, and assessment of system safety [2]. The load forecast error produces high extra costs: if the load is underestimated one has extra costs caused by the damages due to lack of energy or by overloading system elements; if the load is overestimated, the network investment costs overtake the real needs, and the fuel stocks are overvalued, locking up capital investment. Consequently, the quality of load forecasts has greatly influenced the economic planning in areas such as generation capacity, purchasing fuel, assessing system's security, maintenance scheduling, and energy transmission [3]. The power load value is determined by several environmental and social factors among which the seasonal and daily profiles are the most influential.

Temperature and air humidity are the primary parameters determining the energy consumption generally and especially in urban residential areas. Working times, holidays, and seasonal behaviour influence the load-time function. All together, the load curve is a nonlinear function of many variables that map themselves into it in an unknown way.

In an inspired paper [4] Prof. Mendel' claims: "Prediction of short time series is a topical problem. Cases where the sample length N is too small for generating statistically reliable variants of prediction are encountered every so often. This form is characteristic of many applied problems of prediction in marketing, politology, investment planning, and other fields." Further he claims: "Statistical analysis suggests that in order to take carefully into account all components the prediction base period should contain several hundreds of units. For periods of several tens of units, satisfactory predictions can be constructed only for the time series representable as the sum of the trend, seasonal, and random components. What is more, these models must have a very limited number of parameters. Series made up by the sum of the trend and the random component sometimes may be predicted for even a smaller base period. Finally, for a prediction base period smaller than some calculated value N_{min}, a more or less satisfactory prediction on the basis of observations is impossible at all, and additional data are required".

Among the fields not mentioned in [4], dealing with really small set of data or "prediction base period", we will discuss here weekly and monthly short-term prediction of electricity loads at suburban level or on the level of a low voltage transformer station. In fact, the amount of data available in this case is large enough to apply any other forecasting method [5,6,7] but looking to the load diagram i.e. weekly (and monthly) load-value curves, we easily recognize that past values of the consumption are not very helpful when prediction is considered. That stands even for data from the previous week (month) and for data from the same week (month) in the previous month (year). Accordingly, we propose the problem of prediction of the load value in the next week (month) to be performed as a deterministic prediction based on very short time series. To help the prediction, however, in an appropriate way, we introduce past values e.g. load for the same week (month) but in previous month (year). That is in accordance with existing experience claiming that every month (week) in the year (month) has its own general consumption profile [5].

The prediction of a time series is synonymous with modelling the underlying physical or social process responsible for its generation. This is the reason of the task difficulty. There were many attempts during the past few decades to propose a solution to the short term load prediction. Among the most comprehensive overviews of

the subject we find [5] and [2]. The methods applied may be categorized based on several aspects. By one categorization we see methods that use the weather information such as temperature and/or humidity as controlling variables or not [9]. On the other side a categorization exists based on the underlying mathematical algorithm used for modelling. From that point of view we first come to statistical methods (like auto-regression and time-series) predicting average values and deviations. Among them, the best known are the simple moving average (SMA) and the exponential moving average (EMA) method for prediction of trend [1,2]. That category includes the autoregressive integrated moving average (ARIMA) method [10] and similar as well. Although these statistical techniques are reliable, they fail to give accurate results when quick weather changes occur which form a nonlinear relationship with daily load [11]. Hence results of statistical methods in presence of such events are not satisfactory as desired. Therefore the emphasis has shifted to the application of various deterministic methods. Among the deterministic methods, one can find a two-fold categorization: parametric based method [6], [12] and, much frequently encountered the artificial intelligence method that is often represented by implementation of artificial neural networks [13].

The idea in our implementation is reminiscent to the substitution of the simple moving average (SMA) by the exponential moving average (EMA) method for prediction of trend [14,15]. The simple moving average is extremely popular among traders, but one argues that the usefulness of the SMA is limited because each point in the data series is equally weighted, regardless of its position in the sequence. It is common opinion that *most recent data is more significant than the older* and should have a greater influence on the final result. That led us into the subject of prediction based on short time series. Our idea is at the same time inspired by the classical deterministic method known as the *k*-nearest-neighbour [12], in which the data series is searched for situations similar to the current one each time a forecast needs to be made. This method asks for periodicity to be exploited that, as already discussed, in our case, may be helpful but not decisively.

Having all that in mind we undertook a project of developing an artificial neural network (ANN) based method that will be convenient for systematic implementation in stationary time series prediction with reduced set of data. Our first results were applied to prediction of environmental as well as technological data and published in [8,16,17]. Analysis as to why neural networks are implemented for prediction may be found in [8]. The main idea implemented was the following: If one wants to create neural network that may be used for forecasting one should properly accommodate its structure.

Following these considerations new forecasting architectures were developed. Namely, prediction is an activity that is always related to uncertainty. One is supposed to have at least two solutions for them to support each other. The structures developed were named Time Controlled Recurrent (TCR) and Feed Forward Accommodated for Prediction (FFAP). Both were implemented successfully for prediction in modern developments in micro electronics [17] as well as in other areas including load prediction on yearly basis [18].

The goal of this paper is to put the new methods into a broader context of implementation of ANNs for short term forecasting of electricity loads on weekly and monthly basis. Namely, the weekly (we will proceed with one term –week- from now one) load curve at a suburban (transformer station) level is influenced by several factors the main being the time of the year. Accordingly a predictor is to be capable to approximate two curves concurrently. To meet that we upgraded our original TCR and FFAP ANN structures to accommodate for implementation in the field of short term electricity load forecasting on hourly basis. The results obtained were published in [19] and [20], for feed-forward and for recurrent ANNs, respectively. Those ideas will now be implemented for weekly and monthly prediction. In addition we here we propose an averaging method that will use both predictions in order to smooth the prediction error so making the final result as dependable as possible. Finally, we propose a method for finding the proper number of hidden neurons in both networks.

The structure of the paper is as follows. After general definitions and statement of the problem we will give a short background related to ANNs application to forecasting. Then we will describe two solutions for possible applications of ANNs aimed to the same forecasting task. Finally short discussion of the results and consideration related to future work will be given.

II. PROBLEM FORMULATION AND SOLUTION

A time series is a number of observations that are taken consecutively in time. A time series that can be predicted precisely is called deterministic, while a time series that has future elements which can be partly determined using previous values, while the exact values cannot be predicted, is said to be stochastic. We are here addressing only deterministic type of time series.

Consider a scalar time series denoted by y_i, i=1, 2, … m. It represents a set of observables of an unknown function, taken at equidistant time instants separated by the interval Δt i.e. $t_{i+1}=t_i+\Delta t$. One step ahead forecasting means to find such a function $\hat{y} = \hat{f}(t)$, that will perform the mapping

$$y_{m+1} = f(t_{m+1}) = \hat{y}_{m+1} + \varepsilon, \qquad (1)$$

where $\hat{y}_{m+1}$ is the desired response, with an acceptable error ε.

The prediction of a time series is synonymous with modeling of the underlying physical or social process responsible for its generation. This is the reason of the

difficulty of the task. There have been many attempts to find solution to the problem. Among the classical deterministic methods we may mention the *k*-nearest-neighbor [21], in which the data series is searched for situations similar to the current one each time a forecast needs to be made. This method asks for periodicity to be exploited that, as already discussed, here is not of much a help.

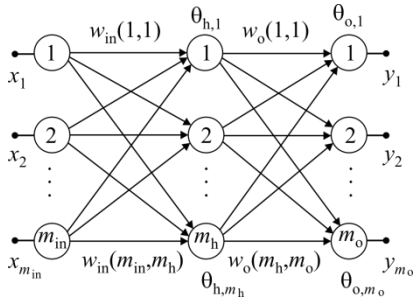

Fig. 1. Fully connected feed-forward neural network with one hidden layer and multiple outputs

In the past decades ANNs have emerged as a technology with a great promise for identifying and modeling data pat-terns that are not easily discernible by traditional methods. A comprehensive review of ANN use in forecasting may be found in [22]. Among the many successful implementations we may mention [23]. A common feature, however, of the existing application is that they ask for a relatively long time series to become effective. Typically it should be not shorter then 50 data points [22]. In the case under consideration it means at least five years backward. This is due to the fact that they all look for periodicity within the data. Very short time series were treated [23]. Here additional "non-sample information" was added to the time series in order to get statistical estimation from deterministic data.

That is why we went for a search for topological structures of ANN that promise prediction based on short time series. In the next, we will first briefly introduce the feed-forward neural networks that will be used as a basic structure for prediction throughout this paper.

The network is depicted in Fig. 1. It has only one hidden layer, which has been proven sufficient for this kind of problem [24]. Indices: "in", "h", and "o", in this figure, stand for input, hidden, and output, respectively. For the set of weights, $w(k,l)$, connecting the input and the hidden layer we have: k=1,2,..., m_{in}, l=1,2,..., m_h, while for the set connecting the hidden and output layer we have: k=1,2, ...m_h, l=1,2,..., m_o. The thresholds are here denoted as θ_{x,m_r} where r=1,2, …, m_h or m_o, with x standing for "h" or "o", depending on the layer. The neurons in the input layer are simply distributing the signals, while those in the hidden layer are activated by a sigmoidal (logistic) function. Finally, the neurons in the output layer are activated by a linear function. The learning algorithm used for training is a version of the steepest-descent minimization algorithm [25]. The number of hidden neurons, m_h, is of main concern. To get it we applied a procedure that is based on proceedings given in [26] but here further developed.

In prediction of time series, in our case, a set of observables (samples) is given (approximately every fifteen minutes) meaning that only one input signal is available being the discretized time [27]. To get the average monthly consumption we averaged the data for every month of the year. According to (1) we are predicting one quantity at a time meaning one output is needed, too. The values of the output are numbers (average power for a period of one month). To make the forecasting problem numerically feasible we performed transformation in both the time variable and the response. The time was reduced by t_0 so that

$$t=t^*-t_0. \tag{2}$$

Having in mind that t^* stands for the time (in weeks), this reduction gives the value of 0 to the time (t_0) related to the first sample. The samples are normalized in the following way

$$y=y^*-M \tag{3}$$

where y^* stands for the current value of the target function, M is a constant (for example M=595.19, being the average monthly consumption for a year).

If the architecture depicted in Fig. 1 was to be implemented (with one input and one output terminal) the following series would be learned: $(t_i, f(t_i))$, i=1,2,....

Starting with the basic structure of Fig. 1, in [16] possible solutions were investigated and two new architectures were suggested to be the most convenient for the solution of the forecasting problem based on short prediction base period. Here, however, having in mind the availability of data related to previous year, these architectures will be properly accommodated.

The first one, named *time controlled recurrent* (TCR) was inspired by the time delayed recurrent ANN. It is a recurrent architecture with the time as input variable so controlling the predicted value. Our intention was to benefit from both: the generalization property of the ANNs and the success of the recurrent architecture. Its structure is depicted in Fig. 2a

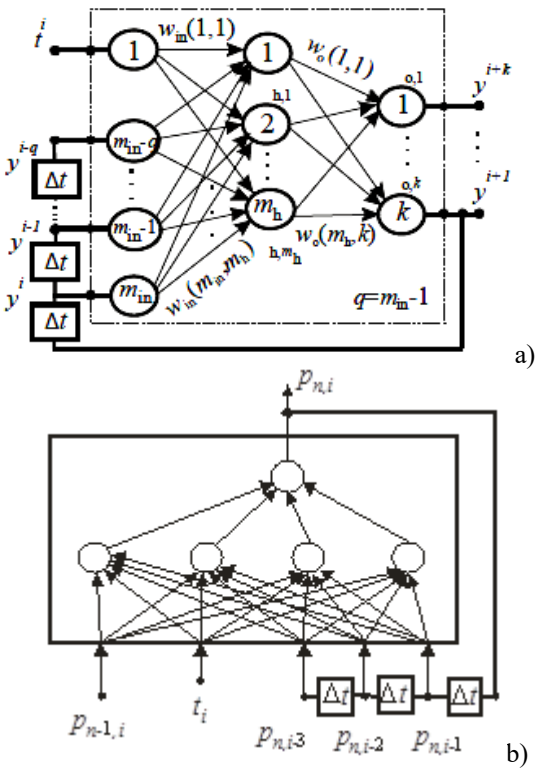

Fig. 2. a) Time controlled recurrent ANN and b) ETCR. b) Extended time cont rolled recurrent ANN

We extend, now, this architecture so that we allow for the values of the power consumption, at a given time per day, but of the same month in the previous year, to control the output.

Hence, the term extended will be added. The resulting architecture is depicted in Fig. 2b. It will be referred from now on to as the Extended Time Controlled Recurrent (ETCR) architecture. Here in fact, the network is learning a set in which the output value representing the average power consumption for a given month in a given year is controlled by the present time and by its own previous instances:

$$p_{n,i} = f(t_i, p_{n,i-1}, p_{n,i-2}, p_{n,i-3}, p_{n-1,i}) \quad i = 1,2,3... \quad (4)$$

Here n stand for the number of the month (in the year). In that way the values indexed with n are from the actual year, while the value indexed n-1 is from the previous year. i stands for the i-th sample in the year selected. The actual value $p_{n,i}$ is unknown and should be predicted. Incrementing i, in fact, means moving the prediction window one step ahead. These quantities are illustrated in Fig. 3. It represents the load curve for a two years. Note the x-axis is reduced to the first week available while the y-axis represents the same curve twice. The upper curve depicts original load values while the lover represents the reduced value (by the average weekly) consumption.

The second structure was named *feed forward accommodated for prediction* (FFAP) and depicted in Fig. 4a. Our idea was here to force the neural network to learn the same mapping several times simultaneously but shifted in time. In that way, we suppose, the previous responses of the function will have larger influence on the $f(t)$ mapping. In this architecture there is one input terminal that, in our case, is t_i. The *Output*3 terminal, or the *future* terminal, in our case, is to be forced to approximate y_{i+1}. In cases where multiple-step prediction is planned *Output*3 may be seen as a vector. *Output*2 should represents the *present* value i.e. y_i. Finally, *Output*1 should learn the *past* value i.e. y_{i-1}. Again, if one wants to control the mapping by a *set* of previous values, *Output*1 may be seen as a vector.

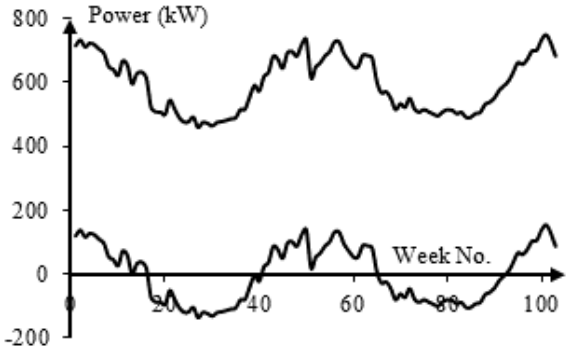

Fig. 3. Average power (top) and its reduced value, by 595.19, (bottom) versus time (weeks)

As an example we may express the functionality of the network as

$$\{y_{i+1}, y_i, y_{i-1}, y_{i-2}\} = f(t_i), \quad i=3,4,... \quad (5)$$

where *Output*1=$\{y_{i-1}, y_{i-2}\}$, meaning that: one future (i+1), one present (i), and two previous (i-1, i-2) responses are to be learned.

It is our experience that the FFAP architectures produces better results than the TCR. Nevertheless, we regularly implement both of them and use the results obtained as reference to each other when choosing the forecast that makes most sense. That allows avoidance of solutions that represent local minima in the optimization process representing the training of the ANN.

In the case of hourly prediction of power consumption we extended the FFAP architecture exactly in the same way as we did with the TCR. In that way for the approximation function we may write the following

$$\{p_{n,i+1}, p_{n,i}, p_{n,i-1}, p_{n,i-2}\} = f(t_i, p_{n-1,i}) \quad i=1.2.3... \quad (6)$$

The new network is approximating the future (unknown) value $p_{n,i+1}$, based on the actual time t_i, the actual consumption $p_{n,i}$, the past consumption values for the given year ($p_{n,i-k}$, k=1,2,3), and the past consumption values

for the same month at the actual time of the previous year ($p_{n-1,i}$). The new architecture is referred to as extended feed forward accommodated for predict ion (EFFAP). It is depicted in Fig. 4b.

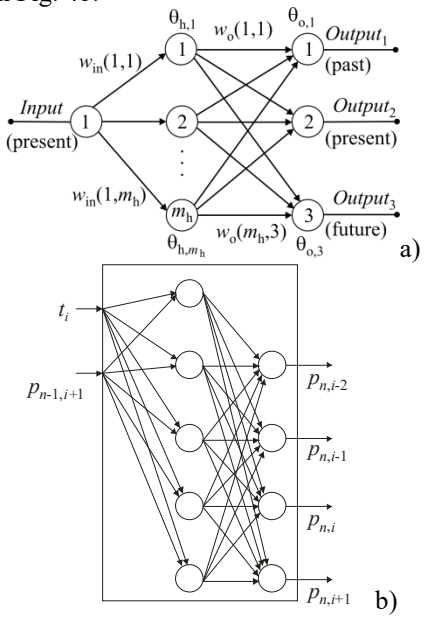

Figure 4. a) Feed forward ANN structure accommodated for predict ion (FFAP), and b) The Extended feed forward accommodated for predict ion ANN (EFFAP) according to (6)

In the next the procedure of implementation of ETCR and EFFAP network will be described. It consists of the following steps.

STEP 1. For a given week (month) (ith week) a training table is constructed for both ANN structures. These constructs are illustrated in Table I and Table II, for the ETCR and EFFAP network, respectively, for i=44.

STEP 2. Both network are repeatedly trained with the same training data but with increased complexity i.e. with increased number of hidden neurons. We start with m_h=3 and end with m_h=10. The number of neurons is chosen to be "small" since the problem under consideration is not a difficult one. One is not to forget that an ETCR ANN, like the one depicted in Fig. 2, having 10 hidden neurons, will have 70 free parameters which is much above the need to extrapolate by one step the curve given in Fig. 3.

STEP 3. To find the proper ETCR and EFFAP number of hidden neurons, the predicted values are compared. Namely, we consider the prediction as a step in darkness and to get an authentic prediction, we think, one needs at least two solutions supporting each other (The well known medical "second opinion"). In that way we choose two among the eight ETCR and eight EFFAP solutions (each from a kind) that are the most similar.

4. Since the ETCR and the EFFAP solutions just chosen are of the same importance, as the final result, we adopt their average.
5. Then we proceed to the next week

III. Implementation Example

The diagram depicted in Fig. 3 is created from the UNITE competition data [27]. Since there are data for two years only we created 24 instances for monthly and 101 instances for weekly consumption as depicted in Fig. 3. Having in mind, however that our method asks for a value of the load for the same month in the previous year, the first 12 instances are to be reserved. Furthermore, to start the prediction we need some values of the previous months. For these reasons we started the prediction with the fourth part of the data i.e. from the 19th month. The weekly prediction started at the end of the first year (last week of December) which, as will be discovered later is of importance for the prediction results.

TABLE I ONE TRAINING SESSION FOR ECTR FOR WEEKLY PREDICTION

Inputs					Outputs
t_i	$p_{n,i-1}$	$p_{n,i-2}$	$p_{n,i-3}$	$p_{n-1,i}$	$p_{n,i}$
45	76.84	86.73	37.08	-113.56	49.92
46	49.92	76.84	86.73	-108.83	97.17
47	97.17	49.92	76.84	-105.85	101.78
48	101.78	97.17	49.92	-80.29	87.01
49	87.01	101.78	97.17	-78.52	121.89
50	121.89	87.01	101.78	-40.11	140.05
51	140.05	121.89	87.01	-4.31	?

TABLE II ONE TRAINING SESSION FOR EFFAP FOR WEEKLY PREDICTION

Inputs		Outputs			
t_i	$p_{n-1,i}$	$p_{n,i-2}$	$p_{n,i-1}$	$p_{n,i}$	$p_{n,i+1}$
44	-113.56	37.08	86.73	76.84	49.92
45	-108.83	86.73	76.84	49.92	97.17
46	-105.85	76.84	49.92	97.17	101.78
47	-80.29	49.92	97.17	101.78	87.01
48	-78.52	97.17	101.78	87.01	121.89
49	-40.11	101.78	87.01	121.89	140.05
50	-4.31	?	?	?	?=$p_{n,51}$

Table I and Table II are examples of the training set for the first prediction. The rest of the training set is obtained by "sliding" down the table of the load as a function of the week number.

TABLE III THE MOST SIMILAR ETCR AND EFFAP SOLUTIONS ON RESTORED ORIGINAL INPUT DATA FOR WEEKLY PREDICTION

t_n	ECTR	EFFAP	Average	Expected

	m_h	(p)	m_h	(p)	(p)	(p)
51	5	746.759	5	736.506	741.633	615.027
52	7	662.406	8	663.523	662.964	647.869
53	3	579.127	9	706.465	642.796	661.6578
54	9	740.493	8	635.385	687.939	683.78
55	10	675.972	5	668.981	672.477	696.83
56	5	697.742	8	698.717	698.23	726.75
57	9	761.235	10	762.086	761.66	726.583
58	6	716.076	6	719.692	717.884	690.366
59	6	670.976	4	687.522	679.249	668.848
60	4	662.313	6	663.963	663.138	649.366

As a result of STEP 3 described in the previous paragraph, Table III was created. While its content is self explainable we will here stress again that among the predictions for a given week, the two most similar were saugth. So, for example, for the 54th week the prediction of the ETCR ANN built by nine hidden neurons and the EFFAP ANN built by eight neurons were the most similar ones. These two were chosen and the average calculated.

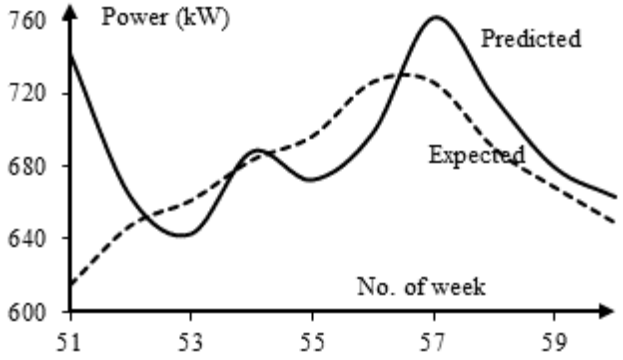

Fig. 5. Visualization of the last two columns of Table III

TABLE IV PREDICTION ERROR FOR WEEKLY PREDICTION

t_i	Error ECTR %	Error EFFAP %	Error Average %
51	-21.4	-19.8	-20.6
52	-2.24	-2.42	-2.33
53	12.5	-6.77	2.85
54	-8.3	7.08	-0.608
55	3.0	4.0	3.5
56	4.0	3.86	3.92
57	-4.77	-4.89	-4.83
58	-3.72	-4.25	-3.99
59	-7.06	-7.60	-7.33
60	-1.99	-2.25	-2.12

Note, to complete the prediction the values produced by (3) were to be restored . That practicaly meant that all entries of Table III were obtained by incrementation by 595.19. Fig. 5 depicts the two last columns of Table III. Namely the expected and the predicted values are drawn together.

Finally, in order to get even better insight into the results, the prediction error was calculated and depicted in Table IV. A graphical representation of Table IV is given in Fig. 6. It is easy to recognize that after escaping from the "fatal" last week of the year, the prediction goes smoothly wit prediction error no larger than 8%.

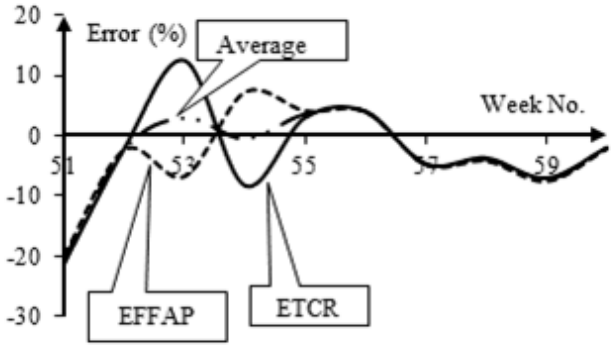

Figure 6. Prediction error (in %) of the ETCR, EFFAP and the averaged solution (Graphical depiction of Table IV)

Table V represents the numerical data used to create Fig. 8.

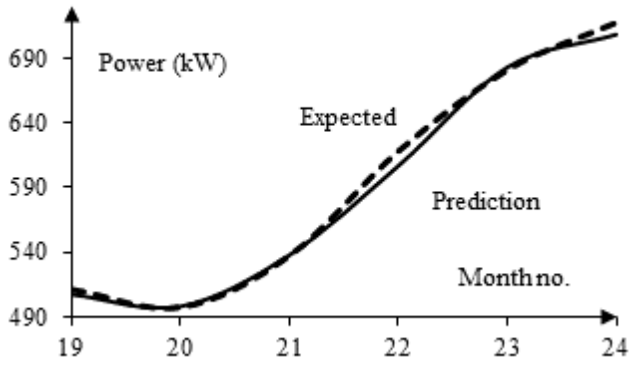

Fig. 7. Visualization of the last two columns of Table IV

After implementation the same procedure to the prediction of the monthly consumption we got the curves depicted in Fig. 7 and Fig. 8, for the consumption and for the error, respectively.

As can be seen the error of the average value compared with the expected one is less than 2% in all six cases.

It is interesting to note that the prediction errors of the ETCR and the EFFAP ANNs are much larger (less than 6%). That means that the worst prediction would never exceed that value. By good luck, however, in this case, cancellation occurred during the computation of the average which led to an extraordinary good result.

TABLE V PREDICTION ERROR FOR MONTHLY PREDICTION

t_i	Error (%) ECTR	Error (%) EFFAP	Error (%) Average
19	1.735	-0.5267	0.604
20	-1.240	0.6625	-0.289

21	4.687	-4.988	-0.151
22	3.051	0.576	1.813
23	-0.506	-0.161	-0.334
24	2.798	-0.335	1.232

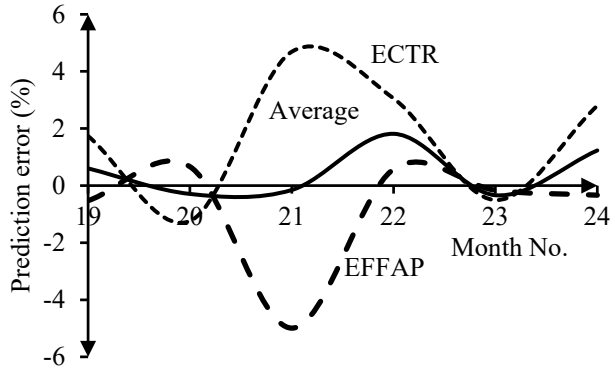

Figure 8. Prediction error (in %) of the STCR, EFFAP and the averaged solution (Graphical depiction of Table V)

IV. Conclusion

One week (month) ahead prediction of suburban average electricity load, based on short time series, was presented. It was shown first that for the subject of short term prediction of electricity load, even though a large amount of data may be available, only the most recent of it may be of importance. That gives rise to prediction based on limited amount of data. We here proposed implementation of some instances of architectures of artificial neural networks as potential systematic solution of that problem as opposed to heuristics that are in use. To further rise the dependability of the predicted data averaging of two independent predictions was proposed. A specific approach to the choice of the number of hidden neurons was implemented. Example was given related to monthly forecasting of the electricity load at suburban level. Prediction was carried out on real data taken the literature. Acceptable prediction errors were obtained.

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Energy – Efficient CMOS Full Adders

Branko Dokić, Miladin Sandić

Abstract - This paper gives a summary of CMOS full-adder cells topologies and their comparison from the aspect of energy efficiency. A special attention is given to Hybrid-CMOS logic style full-adders. Logic delay and power consumption are analyzed. These topologies are found in three CMOS operating modes: standard, mixed or hybrid and sub-threshold mode. These characteristics are obtained by application of the PSPICE and the parameters of 180nm technology.

Keywords - Full-adder, CMOS logic design, logic delay, low-power.

I. Introduction

Two opposed demands are often posed before a designer of a digital system: to achieve greater data process speed and lesser electrical energy consumption. A compromised solution is in one of two following strategies: lesser consumption at given frequency range or greater frequency at given maximum electric energy consumption. Therefore an energy efficient system often involves a system designed in accordance with the demands of one of two mentioned strategies. Such project is often called optimal. Optimal project includes decomposition of system architecture, a good choice of basic cell and module topology and a good choice of technology. A designer is therefore required to possess excellent knowledge of components, basic logic cell topologies and modules, and system architecture.

The strategy of minimal consumption in a given frequency range is bounded by data process speed, and also by a presented project task, technology, topology of cells for the synthesis of logic functions and by accuracy. As this includes five specifications, which can be illustrated with the fingers of the hand, this strategy is also known as “the low-power hand.” [1]

The optimization of consumption is therefore multidimensional demand which includes optimization in each design phase of a complex integrated circuit or a digital system. The greatest economization of electrical energy is realized during the opening phases of design, when the project is at the drawing board.

The first section of this paper, through several topologies of the CMOS full adder, shows how important is a good knowledge of logic possibilities of the selected technology during the design of the optimal system. Naturally, not all of the possible logic options are analyzed here, but only some representative groups.

As previously emphasized, an energy efficient system of a given technology and topology is primarily influenced by operating speed and electrical energy consumption. In CMOS technology, these two parameters depend on operating mode of CMOS logic and on the relation between supply voltage V_{DD} and the threshold voltage V_t of the MOS transistor. Afterwards we will consider the threshold voltage of nMOS and pMOS transistor as equal by absolute value, i.e. $V_{tn} = |V_{tp}| = V_t$. When $V_{DD} > 2V_t$ CMOS logic circuits are operating in the standard or conventional mode, and if $V_{DD} < V_t$ then they are in the sub-threshold CMOS operating mode. There is also the mixed or hybrid CMOS mode in the region $V_t < V_{DD} < 2V_t$ [2].

The possibilities and limitations of each CMOS operating mode are shown on the example of hybrid topology of 4-bit ripple-carry adder. The characteristics of logic delay and power consumption are obtained by the application of PSPICE program and 180 nm CMOS technology parameters.

II. Models of static CMOS adders

The basic structure of the full 1-bit adder consists of two half adder and one 2-input OR circuit. It is described by the following analytic model:

$$s_i = a_i \cdot \oplus b_i \oplus c_i$$
$$c_{i+1} = a_i \cdot b_i + (a_i \oplus b_i)\, c_i \qquad (1)$$

where a_i and b_i are both input bit operandi; c_i and c_{i+1} are input and output carry-signal respectively, and s_i is the sum. The optimal synthesis of the equation implies a minimal number of MOS transistors of the selected topology of the basic CMOS logic cells (CMOS logic).

A. Conventional logic

It is well known that the conventional logic is based on the application of trasnsistor network with one pair of nMOS and pMOS transistors on each input. It can thereby be dual or symmetrical. In the first case nMOS and pMOS networks are dual, and in the second they are symmetrical. Dual networks are standard, and symmetrical ones are applicable only in specific cases, such as binary adders.
Optimal synthesis of the full adder with the conventional logic stems from a modified system of equations of the sum

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s_i and carry c_{i+1}:[3]

$$\begin{aligned} s_i &= a_i b_i c_i + (a_i + b_i + c_i)\overline{c}_{i+1} = \overline{s}_{in} \\ c_{i+1} &= a_i b_i + (a_i + b_i)c_i = \overline{c}_{(i+1)n} \end{aligned} \quad (2)$$

The function of nMOS networks of complementary functions $\overline{s}_i$ and $\overline{c}_{i+1}$ are determined by (2), and the corresponding dual pMOS networks, obtained by replacing logic operators "·" and "+" in (2), which yields:

$$\begin{aligned} \overline{s}_{ip} &= (a_i + b_i + c_i)\cdot(\overline{c}_{i+1} + a_i b_i c_i) \\ \overline{c}_{(i+1)p} &= (a_i + b_i)\cdot(c_i + a_i b_i) \end{aligned} \quad (3)$$

Dual networks (2) and (3) have 12 inputs and as much of CMOS transistor pairs. The complements $\overline{s}_i$ and $\overline{c}_{i+1}$ signals are at the network outputs, so two more inverters would be necessary for generating s_i and c_{i+1} functions.

The output adder functions can also be implemented in symmetrical networks of CMOS transistors.[4] Since in binary algebra $a_i\, b_i\, c_i\, (a_i + b_i + c_i) = a_i\, b_i\, c_i$ or $a_i\, b_i\, (a_i + b_i) = a_i\, b_i$, the functions of pMOS networks are identical to (2), i.e. $\overline{s}_{ip} = \overline{s}_{in}$ and $\overline{c}_{(i+1)p} = \overline{c}_{(i+1)n}$.

Symmetrical or mirror adder possess the same number of MOS transistors (24) as dual adder network. The advantage of symmetrical adders is that their property of symmetry guarantees equal rise and fall time of signals s_i and $\overline{c}_{i+1}$. On the other hand, the number of serial pMOS transistors in symmetrical sum and carry networks is reduced by one, which increases their speed.

B. XOR – XNOR – MUX model

The sum and carry functions (1) of the full adder can be presented in the following form:

$$\begin{aligned} s_i &= p_i \oplus c_i \\ c_{i+1} &= \overline{p}_i a_i + p_i c_i \end{aligned} \quad (4)$$

considering that $\overline{p}_i a_i = a_i b_i$, where

$$p_i = a_i \oplus b_i \quad (5)$$

is the carry propagate signal. The adder logic scheme according to (4) consists of two XOR circuits and multiplexer 2/1 (Fig.1). The propagate signal p_i is applied to multiplexer select input.

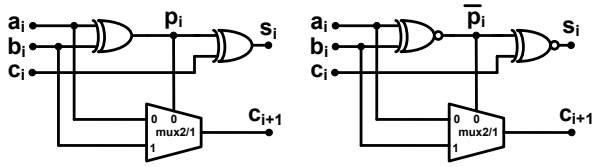

Fig. 1. XOR – MUX (a) and XNOR – MUX full adder logic schemes (b)

The XNOR logic circuits can be applied instead of XOR. This stems from the following logic model of the full adder:[5]

$$\begin{aligned} s_i &= \overline{\overline{p}_i \oplus c_i} \\ c_{i+1} &= \overline{p}_i a_i + p_i c_i \end{aligned} \quad (6)$$

This model possesses the XNOR logic circuits, instead of XOR (Fig.1b). The complement of propagate signal p_i is the multiplexer 2/1 select input.

C. Pass-transistor logic

The basic logic cell of pass-transistor logic is the transmission gate which consists of of two CMOS transistors connected in parallel. The synthesis of XOR, XNOR and MUX 2/1 functions with the transmission gates is shown in Fig. 2. [6] The sources of CMOS transistors Mn and Mp are applied to signal lines *b* and $\overline{b}$ (Fig. 2 *a* and *b*), instead to power supply lines. Weather the XOR – MUX or XNOR – MUX topology is applied, we will get the full adder with 18 transistors in total, including inverters for complements $\overline{b}$ and $\overline{p}$.

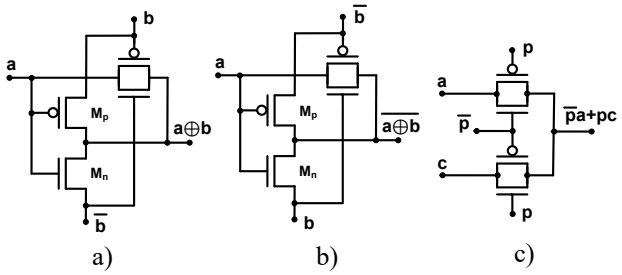

Fig. 2. Pass-transistor topologies of XOR (a), XNOR (b) and MUX 2/1 (c) circuits

D. Differential Cascade Voltage Switch Logic – DCVSL

DCVSL consists of two complementary nMOS networks with complement excitations cross-connected by two pMOS transistors [6] (Fig. 3a). Compared to the conventional CMOS logic, DCVSL has greater speed because the pMOS transistors in the transistor logic network are replaced by nMOS ones of the smaller area. Here the pMOS transistors are providing the full logic

change of the output signal from 0 to V_{DD}. The disadvantage of this logic lies in relatively great number of nMOS transistor and in the need for complement signals. The number of nMOS transistors can be decreased if there is a possibility of two networks sharing a transistor, like in XOR/XNOR circuits (Fig. 3a). Additional decrease in transistors is obtained by applying the source to signal lines, instead to the ground, as suggested in [5] (Fig. 3b).

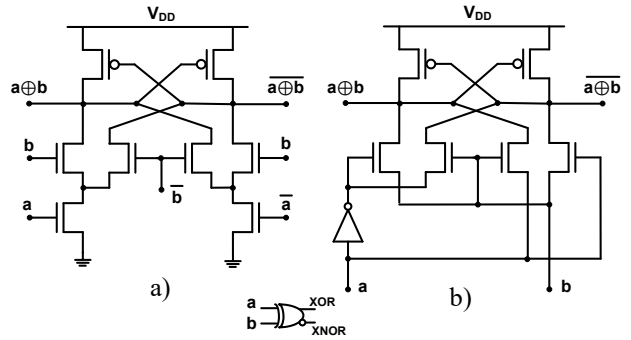

Fig. 3. DCVSL XOR/XNOR circuits

III. 4-BIT RIPPLE-CARRY ADDER

This chapter analyses the consumption and delay characteristics of the 4-bit ripple-carry adder. As already known, it consists of four 1-bit adders interconnected trough input and output carry signals. The topology of hybrid full adder [5] (Fig. 4) based on XOR-XNOR-MUX models is applied in this paper. The XOR-XNOR DCVSL. circuit for generating p_i and $\overline{p}_i$ signals is used. The module for generating the sum is a transmission-function implementation of the XNOR logic. The carry signal is generated by the hybrid-CMOS MUX 2/1, which is consisted of symmetrical logic circuits with inputs a_i and b_i and a transmission gate with input $\overline{c}_i$. The static inverters on outputs s and c_o provide good driving capabilities.

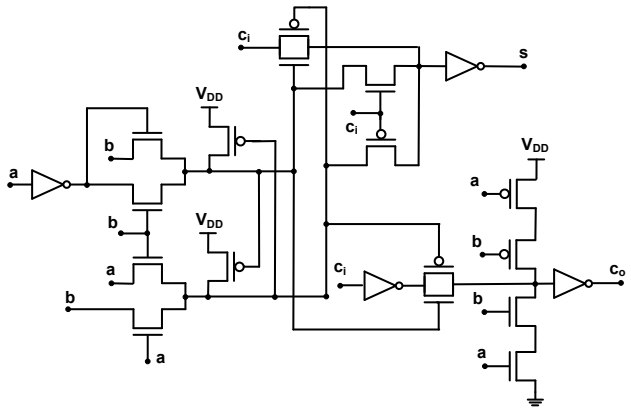

Fig. 4. Hybrid full adder

A. SPICE simulation

The characteristics of logic delay and electrical energy consumption of a 4-bit parallel repple carry adder with hybrid logic of 1-bit adder are obtained with SPICE analysis by the implementation of program package ORCAD 16.3 (Cadence Design Systems) and with 180nm CMOS technology. The threshold voltages of all MOS transistors are $Vt = Vtn = |Vtp|$ = 370mV, and channel width of nMOS and pMOS transistors, respectively, Wn = 0.3µm and Wp = 0.8 µm. The analysis includes all three CMOS operating modes while some other authors only provide the characteristics of the conventional mode.

As previously stated, there are three CMOS operating modes: sub-threshold ($V_{DD} < V_t$), mixed or hybrid ($V_t < V_{DD} < 2V_t$) and conventional or standard ($V_{DD} > 2V_t$). For that reason we have simulated the characteristics in the voltage range $200mV \leq V_{DD} \leq 2V$. Hence, within the range of $200mV \leq V_{DD} < 370mV$ is the sub-threshold mode, within $370mV < V_{DD} < 740mV$ is the mixed mode, and within $740mV < V_{DD} \leq 2V$ is the standard CMOS mode.

Fig. 5 shows the dependency of logic delay on supply voltage and on load capacitance C_L, as a parameter applied on the output carry node. In the sub-threshold region logic delay is exponentially decreasing function of the supply voltage. For C_L = 1f F, $td \approx$ 20µs at V_{DD} = 200mV, and $t_d \approx$ 0.9µs at V_{DD} = 350mV. In the mixed and standard CMOS mode $td \sim 1/V_{DD}$. For C_L = 1fF, in the mixed mode $t_d \approx$ 0.3µs at V_{DD} = 400mV, and $td \approx$ 5.5ns at V_{DD} = 700mV, while in the standard mode $t_d \approx$ 3ns at V_{DD} = 800mV and $t_d \approx$ 0.6ns at V_{DD} = 2V.

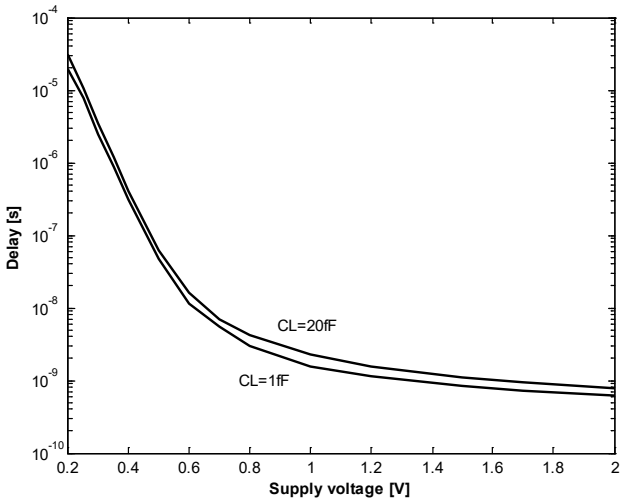

Fig. 5. Logic delay versus supply voltage

The electrical energy consumption as a function of supply voltage is shown in Fig.6. The total consumption in the sub-threshold mode is changing from 40pW to about 0.4nW, in the mixed mode from about 0.8nW to approximately 7.5nW, and in the conventional mode from about 10nW to approximately 600nW.

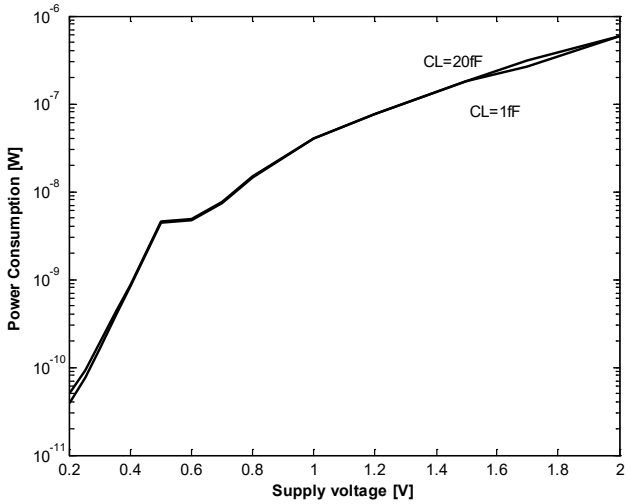

Fig. 6. Power consumption versus V_{DD}

Fig. 7. shows the consumption dependency on the logic delay. The scale of both axis is logarithmic. As expected, the smaller logic delay is, the consumption is bigger and vice versa.

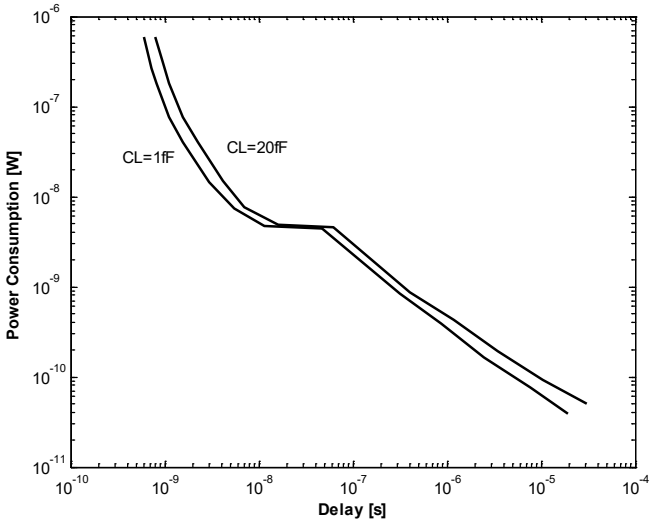

Fig. 7. Power consumption versus logic delay

The best measure of energy efficiency is the power-delay product–PDP (Fig.8). As shown in Fig. 8, the minimum PDP value is in the mixed CMOS mode.

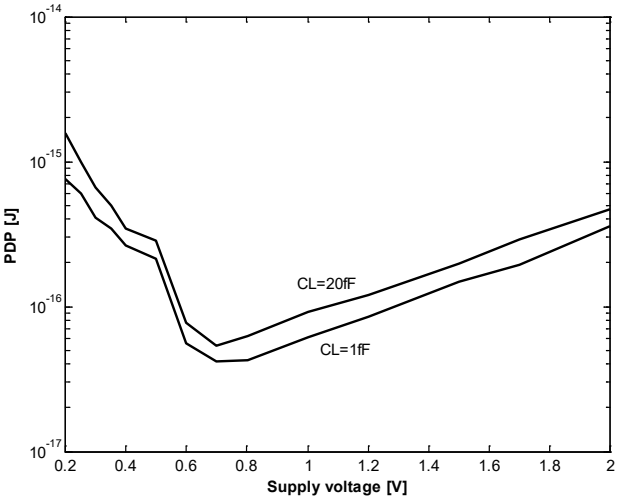

Fig. 8. Power delay product versus V_{DD}

III. CONCLUSION

The adders with pass transistor and DCVSL logic show better characteristics of consumption and delay times than those with conventional logic. The best results are obtained by implementing the hybrid logic. The electrical energy consumption of the hybrid 4-bit parallel ripple-carry adder is ranging from several dozen do several hundred *pW* in the sub-threshold mode, and around ten *nW* to several hundred *nW* in the standard CMOS mode. The logic delay in the sub-threshold mode is in the *μs* range, and within *ns* in the conventional mode. The minimal value of power-delay product in the function of supply voltage is in the mixed mode.

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Periodic Steady State Simulation of Mixed-Signal RF Circuits

Dušan N. Grujić, Mihajlo Božović, Pavle Jovanović, Milan Savić, and Lazar Saranovac

Abstract – Advances in CMOS technology have enabled the use of digitally assisted RF concepts for significant performance improvement and cost reduction. As a result, periodic steady state simulation of mixed-signal RF circuits is becoming increasingly important. Standard mixed-signal simulators only support transient analysis, while RF simulators are not supporting digital simulation and have problems with memory elements. In this paper we propose a solution for periodic steady state simulation of mixed-signal RF circuits. Advantages, limitations and pitfalls of the proposed solution are presented. The proposed solution is demonstrated on example of dynamic performance improved RF D/A converter simulation. Significant improvement of SFDR shows the importance and potential of digitally assisted RF circuits, and the ability to efficiently simulate them.

Keywords - periodic steady state, mixed-signal, RF

I. Introduction

Circuit simulation requires a delicate balance between accuracy, simulation time and resources. Higher level abstraction methodologies and tools have been developed to cope with ever growing complexity, while preserving the required accuracy and important metrics. These concepts have been adopted in digital design decades ago, where an enormous number of gates made a transistor level simulation impractical, and in many cases impossible. Higher abstraction levels have been widely adopted in analog design much later, with the advent of Verilog-A [1]. Further increase in simulation efficiency has been achieved by the development of specialized types of simulation, such as periodic steady state (PSS) for RF circuits, and simulators, such as mixed-signal simulators.

Increased use of digital gates in RF circuits, e.g. [2], has created the need for PSS simulation of mixed-signal circuits. Currently available mixed-signal simulators are not capable of PSS simulation, while the PSS analysis does not support simulation of digital circuits “out of the box”, and suffers from hidden state problem [3].

This paper reviews the limitations of mixed-signal and PSS simulations in Sec. II, and proposes a solution for the functional mixed-signal PSS simulation in Sec. III. Demonstration of proposed solution is presented in Sec. IV. Conclusion and final remarks are given in Sec. V.

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II. Mixed-Signal and Periodic Steady State Simulation Limitations

Mixed-signal simulation is performed by coupling analog and digital simulators with A/D and D/A converters, and simulating with the common time step control, as shown in Fig. 1. At each time step analog simulator uses the Newton-Raphson method to solve the non-linear circuit, while the digital simulator performs an event-driven simulation of the compiled Verilog/VHDL/SystemC or mixed-language design. This way both analog and digital simulators can generate events and schedule new time steps for simulation.

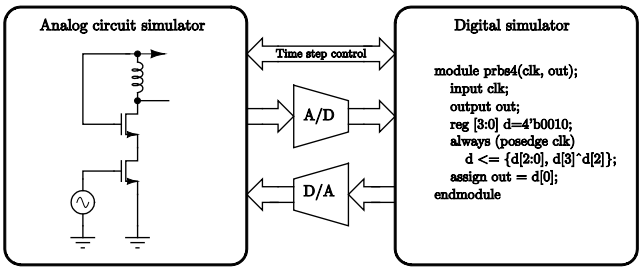


Fig. 1. Analog and digital simulator coupling in mixed-signal simulation

Analog simulator time step is determined by local truncation error (LTE) algorithm and scheduled breakpoints, e.g. by independent sources. Digital simulator can schedule a new time step in two ways: generating an event by behavioral code, and by simulating the propagation delay. The important difference is that behavioral code can generate events on its own, without external stimuli, while the propagation delay generates new events only on external stimuli. If the digital design is synthesizable, it cannot generate events without external stimuli. Furthermore, if a functional model is simulated there are no propagation delays, and the digital simulator cannot schedule new time points at all. Therefore, time step of a mixed-signal simulation containing a synthesizable functional digital design is determined solely by the analog simulator. Digital simulator outputs are only evaluated at time points determined by the analog simulator.

Mixed-signal simulation is efficient, but has its drawbacks, both technical and practical. From the practical point of view, correct setup of mixed signal simulation is all but trivial. There is a cost issue as well, since licenses for both analog and digital simulators are needed.

From a technical point of view, mixed-signal simulation is severely limited, since it only supports transient, AC and linear noise simulations. Transient simulation impedes the analysis of PSS response of RF circuits in several ways:

- Long simulation time might be needed for stiff circuit to enter steady state [4],
- Detection of steady state can be difficult,
- Even when the steady state is reached and detected, the problem of calculating the spectrum remains. Non-uniform time step is not suitable for FFT, but using a fixed time step might skip important transitions, introduce artificial jitter, violate the tolerance settings, or prohibitively prolong the simulation time,
- Large signal steady state transfer functions and noise folding cannot be calculated.

These drawbacks were exactly the motivation for the development of specialized PSS analysis. The usefulness of transient-only mixed-signal simulation of RF circuits is limited to functional verfication.

PSS simulation is suitable for analysis of RF circuits, but does not support the simulation of digital circuits "out of the box". The problem of digital circuits in PSS simulation is not simulator specific, but is related to the mathematical formulation of shooting methods used to determine the steady state, and the inherent hidden state problem [3].

Hidden state problem can be alleviated by exposing the memory element variable to the analog solver by making it an electrical quantity, e.g. charge on a capacitor. Such approach has been taken in [3] for making Verilog-A models of D flip-flop and frequency counter suitable for PSS simulation. However, this approach has two drawbacks:

- Method is not general, and requires case by case consideration,
- Even if all of the memory element models are available in Verilog-A, each instance increases the size of circuit matrix. Having in mind that digital circuits can easily have thousands of memory elements, simulation time and memory requirements might be unacceptable.

In principle, limitations of mixed-signal and PSS could be solved by simulating the complete design on a transistor level. However, this would result in prohibitively long simulation time and memory usage, and possibly convergence difficulties, due to excessively large number of transistors. A solution which allows the use of PSS analysis and has the efficiency of mixed-signal simulation is proposed in the next Section.

III. Proposed Solution

In a mixed-signal simulation, synthesizable digital circuit without propagation delays (functional model) does not generate new time points, and is evaluated only at time points determined by the analog simulator. This fact eliminates the need for event scheduling and notion of time in the digital simulator, greatly simplifying its design. Such a simulator can be generated from Verilog code by using an open source tool Verilator [5][6][7].

Verilator generates a digital simulator in C++ of a given module written in synthesizable subset of Verilog language. It has been successfully used in industry for generating cycle-accurate microcontroller models [8]. Simulator generated by Verilator does not have an event scheduler, and the outputs are evaluated only when requested, making it a perfect fit for a functional mixed signal simulation of synthesizable Verilog code. Cadence Spectre circuit simulator allows the use of user-defined C functions in Verilog-A modules. This feature can be used as an interface to digital simulator generated by Verilator.

Usability of synthesizable digital circuit without propagation delays requires some justification. The requirement that a digital circuit should be synthesizable is not a restriction, since the simulated circuit is intended for implementation at later stages of design. Fixed propagation delays can be implemented in A/D and D/A converters, so the requirement for functional model are also not too restrictive.

Proposed solution for the PSS simulation of mixed signal RF circuits is shown in Fig. 2. Notice that there is no time step synchronization, which is a mayor difference from the setup shown in Fig. 1. Circuit simulator sees the wrapper Verilog-A module, which performs A/D and D/A conversion and provides interface to the digital simulator. Module inputs are sampled by a simple A/D converter with a small hysteresis to avoid oscillations during Newton-Raphson iterations, and digital outputs are evaluated at every time step.

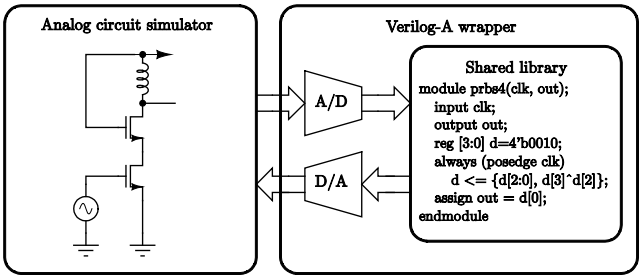


Fig. 2. Proposed solution for periodic steady state mixed-signal simulation

The process of generating the shared library and Verilog-A interface for a given Verilog module has been fully automated by a tool written in Python, called v2va (Verilog to Verilog-A). The tool parses the Verilog module hierarchy by invoking the Verilog-Perl scripts [9], generates the required C++ and Verilog-A wrappers from templates, invokes the Verilator, compiles the generated code and links all of the object files to a shared library, which can be used by Cadence Spectre circuit simulator.

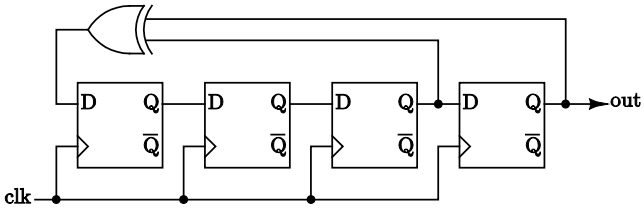
At this point a question emerges: what happened to hidden states? A short answer would be: they are still

present, but are now *very well* hidden states. A bit longer explanation is that the circuit simulator has no means of determining whether memory elements (hidden states) exist, since they are completely implemented in a shared library. As far as the circuit simulator is concerned, there are no hidden states, since it cannot see them. Implementation of memory elements outside of scope of analog solver also means that the circuit matrix size is independent of number of memory elements in digital block, and scales with the number of outputs instead.

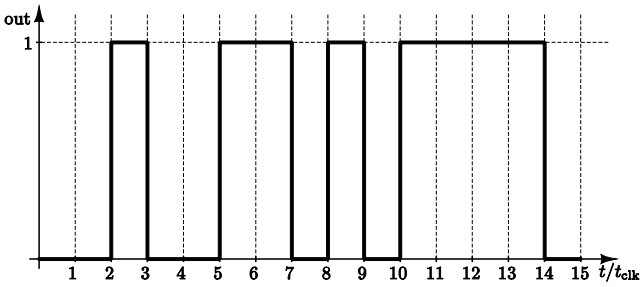
Hiding hidden states from simulator has its pitfalls. Consider a four bit pseudo-random bit sequence (PRBS) generator, shown in Fig. 3a, implemented as maximum length linear feedback shift register with a characteristic polynomial:

$$f(x) = x^4 + x^3 + 1. \tag{1}$$

Generated bit sequence, shown in Fig. 3b, has a period of 15 clocks, so it is expected that the PSS simulation converges with a period of $T = 15t_{\text{clk}}$, which can easily be confirmed by running a simulation.



a) Schematic of four bit PRBS generator



b) Output waveform

Fig. 3. Four bit PRBS generator example

However, simulation also converges for periods of

$$T_{\text{false}} = \{1, 3, 4, 7, 9, 14\} t_{\text{clk}}, \tag{2}$$

because the periodicity condition $v(0) = v(T)$ holds for all signals visible to the simulator as well. False convergence does not arise due to a simulator bug, but due to extra states in digital model which are not visible. The same circuit with output ports at all flip-flop outputs does not exhibit false convergence, i.e. converges only for a period of 15 clocks.

To prevent false convergence, all memory element outputs should be visible to the simulator by connecting them to module output ports. This way the periodicity check is performed by the simulator, but might not be practical due to large number of signals.

To check whether false convergence has occurred, the PSS simulation results should be exported, and the digital simulation should be performed with exported stimuli. If false convergence has occurred, some of internal digital signals will have different values at the start and the end of simulation. This check can be automated with a few scripts.

IV. Periodic Steady State Mixed-Signal Simulation Example

Advances in CMOS technology have resulted in expansion of digitally assisted RF circuits, offering unprecedented levels of performance. Direct RF sampling mixer [2] and dynamic element matching performance improved RF D/A converter [10] demonstrate the benefits of digitally assisted RF circuits. RF D/A converter will be used as an example for the PSS mixed-signal simulation demonstration.

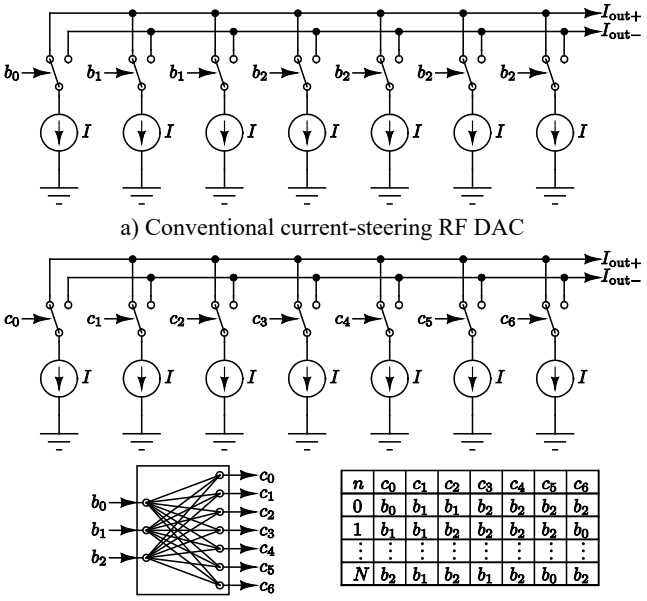
Transistor matching requirements for a Nyquist rate current-steering digital to analog converters are set by the number of bits and expected yield [11]. As the number of bits increases, both unit transistor area and the number of transistor increase, becoming prohibitively large. Various calibration techniques [12][13] have been developed to relax the matching and area requirements. For a special case of RF D/A converter, dynamic performance, such as spurious-free dynamic range (SFDR), is of primary importance. This insight can be used to significantly reduce the chip area, as shown in [10].

Current-steering D/A converter output can be thought of as a sum of desired signal and spurious response generated by mismatch. Spurios response amplitude is determined by the mismatch current, while the number of spurs and their frequencies are determined by the repetition rate and pattern of data bit.

In a conventional binary weighted current-steering D/A converter data bit always controls the same current source, as shown in Fig. 4a. Any mismatch in current source current will produce a spurious response determined by data bit repetition rate and pattern. Spurious response can be reduced by increasing the transistor size to improve matching, or by employing an elaborate calibration scheme, which might require auxiliary circuits.

Randomized dynamic element matching current steering D/A converter principle of operation [10] is shown in Fig. 4b. Each data bit controls the number of current sources corresponding to its binary weight, but in contrast to conventional architecture, the current sources are dynamically assigned at each clock cycle by a predetermined algorithm, usually in a pseudo-random manner. This way the current source, and also its mismatch current, is not controlled by a specific data bit, but is pseudo-randomly assigned to all data bits. Pseudo-random assignment to data bits breaks the repetitive patterns and

spreads the spectral components due to mismatch currents, effectively reducing spurs and increasing SFDR.



a) Conventional current-steering RF DAC

b) Randomized dynamic element matching current-steering RF DAC

Fig. 4. Conventional and RDEM current-steering RF DACs

Randomized dynamic element matching technique significantly relaxes the current source matching requirements, leading to greatly reduced chip area, as demonstrated in [10]. The technique relies heavily on digital circuits, such as pseudo-random number generator and multiplexer matrix for data bit routing, making it an ideal candidate to demonstrate the effectiveness of proposed solution for PSS mixed-signal simulation.

A 10 bit randomized dynamic element matching RF D/A converter, similar to the one from [10] and shown in Fig. 5, has been designed in 65 nm CMOS for demonstration purposes. Eight MSB bits have been assigned to two four bit rotation-based binary weighted D/A converters, while the remaining two LSB bits have been assigned to conventional D/A converter. Data bits have been expanded at inputs of barrel shifters and a buffer, according to their binary weight.

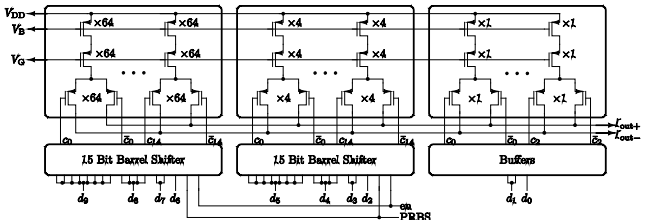


Fig. 5. Designed 10 bit randomized dynamic element matching RF D/A converter schematic

Current sources and current-steering differential pairs have been designed on a transistor level to allow Monte Carlo simulations with foundry-provided models, and to capture the spectral components originating from switch charge injection. Unit current source transistor area has been chosen for drain current mismatch standard deviation of 5%, which corresponds to 3 bit macthing. Transistor W/L was chosen for 250 mV overdrive at nominal 10 µA drain current.

Data multiplexers and 12 bit PRBS generator have been designed as Verilog modules and compiled with v2va tool. Each of four bit D/A converters' data randomizers have been designed as 15 bit four stage barrel shifters, so only right or left rotations of data bits are possible. Data randomizers have an enable input to control whether data bits are rotated or not. When enable bit is set to 0, the converter is a conventional D/A converter, while setting enable to 1 activates the randomized dynamic element matching. To avoid false convergence, all flip-flop outputs of PRBS generator are visible to the analog simulator.

For the purpose of testing the D/A converter, 10 bit digital look-up table sine generator was designed in Verilog. The period of 12 bit PRBS generator is 4095 clock cycles, and the sine generator was designed to have the same number of look-up table entries. To ensure signal coherence [14] and to reduce the impact of repetitions in quantization noise, which result in quantization noise spurs, the number of sine wave periods should be coprime to the total number of waveform samples. Since $4095 = 3^2 \cdot 5 \cdot 7 \cdot 13$ is a composite number, choosing the number of sine wave periods not divisible by 3, 5, 7 and 13 ensures the signal coherence. The digital sine generator was designed to have 127 periods in 4095 samples, which satisfies the coherence condition. Clock frequency was set to 1 GHz.

Although the generated input signal is a sine wave, output spectrum is expected to have significant spurs due to mismatch of transistors in current mirrors. To determine the spurious response due to mismatch, ten runs of Monte Carlo simulation were run. Worst case SFDR without randomized dynamic element matching was in the 7th iteration, is shown in Fig. 6. The 7th iteration simulation was repeated with randomized dynamic element matching, and the results are shown in Fig. 7.

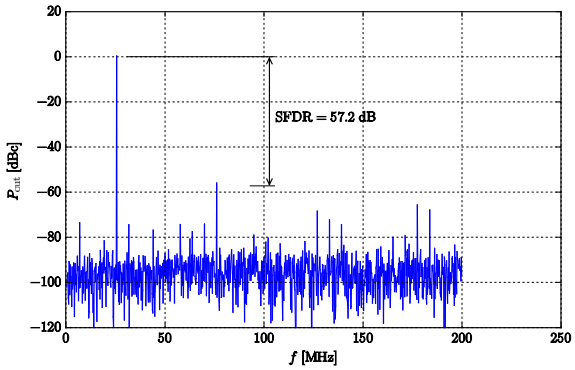


Fig. 6. Worst case SFDR without randomized dynamic element matching in ten Monte Carlo runs

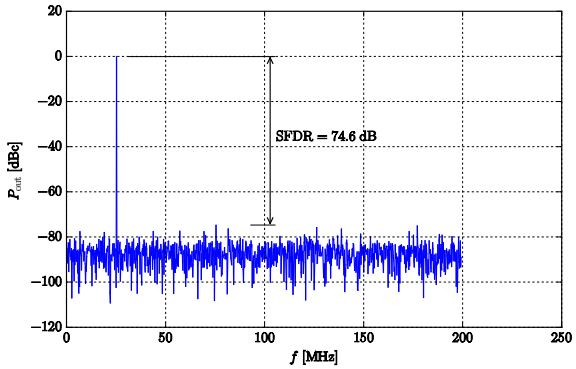


Fig. 7. SFDR improvement with randomized dynamic element matching

Without randomized dynamic element matching, SFDR of 57.2 dB can be achieved with chosen transistor size, which is not adequate for a 10 bit D/A converter. By enabling the randomized dynamic element matching, SFDR is improved to 74.6 dB – an improvement of 17.4 dB. SFDR of 74.6 dB is adequate for 10 bit D/A converter.

The importance of mixed-signal approach can be seen from the reduction in the number of transitors. Simulated circuit has approximately 150 transistors. A single PSS simulation lasts about 20 minutes, requiring 4 GB of memory. It is estimated that two four state 15 bit barrel shifters and a 12 bit PRBS generator would require 1500 transistors for implementation, leading to tenfold increase. Apart from sheer number of transistors, number of time points would be significantly increased, since all of the internal signal propagation would have to be simulated. This would render even a single PSS simulation infeasible.

V. Conclusion

Conventional mixed-signal simulators can only perform basic types of simulation, such as transient, AC and linear noise analysis. PSS-capable simulators do not support digital simulation, and cannot simulate circuits with hidden states. In this paper, we have proposed a solution based on compiling a digital design written in synthesizable subset of Verilog into a shared library with Verilator, and making a Verilog-A wrapper for simulator interface. The proposed solution might exhibit false convergence, which can be prevented and/or detected. The proposed PSS mixed-signal simulation flow has been demonstrated on dynamically matched RF D/A converter, where it was clearly shown that SFDR can be significantly improved by employing digitally assisted techniques.

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Method of Statistical Timing Analysis with Uncertainty

Nazeli Melikyan

Abstract **–** Static timing analysis is a critical step in design of digital integrated circuits. Technology and design trends have led to significant increase in environmental and process variations which need to be incorporated in static timing analysis. This paper presents a new static timing analysis technique considering uncertainty. This new method is more efficient as its models arrival times as cumulative density functions and delays as probability functions.

Keywords – static timing analysis, uncertainty, density function.

I. Introduction

Static timing analysis (STA) is critical to the measurement and optimization of the circuit performance before its manufacture.

The timing or performance of the chip is heavily dependent on the manufacturing process variations (e.g. Vt, Length, etc.) and design environment variations (e.g. VDD and temperature variations, noise impact on timing, etc.). As the feature sizes decrease, the ability to control the manufacturing spread or accuracy of a given feature size is also decreasing. Along with increased process variations, the uncertainty caused by design is also increasing. The increase of uncertainty in design is caused by increase of power supply and temperature variations and interconnect loading uncertainty such as coupling noise impact on timing.

Design variations or uncertainty in static timing analysis is typically handled in two broad ways. The first set of techniques handle variations by worst casing the circuit response. In such a scenario, static timing is performed at various design corners (e.g. fast, slow and nominal design corner).

Another method to handle variations in timing is to perform statistical timing analysis [1,2].

This paper presents a new statistical timing analysis technique. The delay and arrival times in the circuit are modeled as random variables. The arrival times are modeled as Cumulative Probability Distribution Functions and the gate delays are modeled as Probability Density Functions. This leads to efficient expressions for both max and addition operations, the two key functions in both regular and statistical timing analysis.

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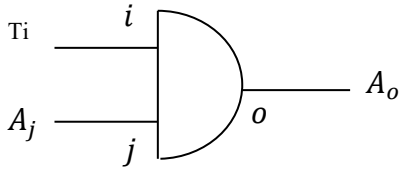
II. Statistical Timing Analysis

The problem in deterministic static timing analysis is to compute arrival times at the output nodes. Arrival times at the input and delay of the gates are specified as deterministic numbers. In case of statistical timing analysis, the arrival times and delays of the gates are specified as distributions. In general, the distribution of delays of the gates can take any form (i.e. normal, uniform, etc.). The problem in statistical timing analysis is to compute distribution of arrival times at the intermediate nodes and the output nodes. Given the required arrival time and distribution of output arrival times, critical paths and slack distributions can be computed for a given probability or confidence level.

Timing analysis is performed by levelizing the circuit. The arrival time at the input is propagated through the gates at each level till it reaches the output. Propagating the arrival times through a gate is a key function in static timing. Consider a two input gate shown in Figure 1.



D_{io}:Delay from Input Node i to Output node o
D_{jo}:Delay from Input Node j to Output node o

Figure 1: A gate with output o and inputs i and j.

In deterministic static timing analysis, arrival time at output node o is given by:

$$A_o = \max(A_i + D_{io}, A_j + D_{jo}) \qquad (1)$$

Computation of max and addition is straight forward in regular timing analysis. In the proposed approach arrival times are modeled as cumulative density functions and the delays are modeled as probability density functions.

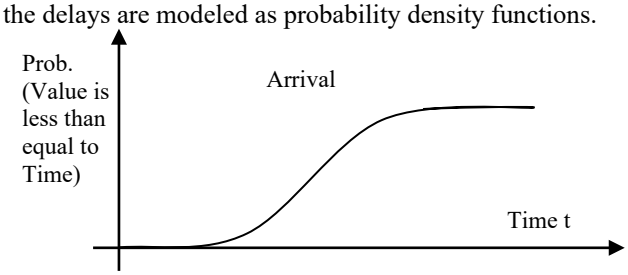


Figure 2: Arrival times are modeled as Cumulative Probability Density Functions.

III. Results

By the proposed method of Statistical Timing Analysis for evaluation the arbitrator circuit has been chosen for the research, which is widely used in electronics (Fig. 3). It is mainly used in asynchronous circuits. During asynchronous requests, the sequence of implementing these requests is selected by means of this circuit. Therefore arbitrator circuit prevents the occurrence of actions at a time when not permitted in the given system. Thus it can be assumed that the arbitrator circuit significantly reduces the probability of having metastability. Preference encoder is used in the arbiter circuit, which enables defining the preferences of requests.

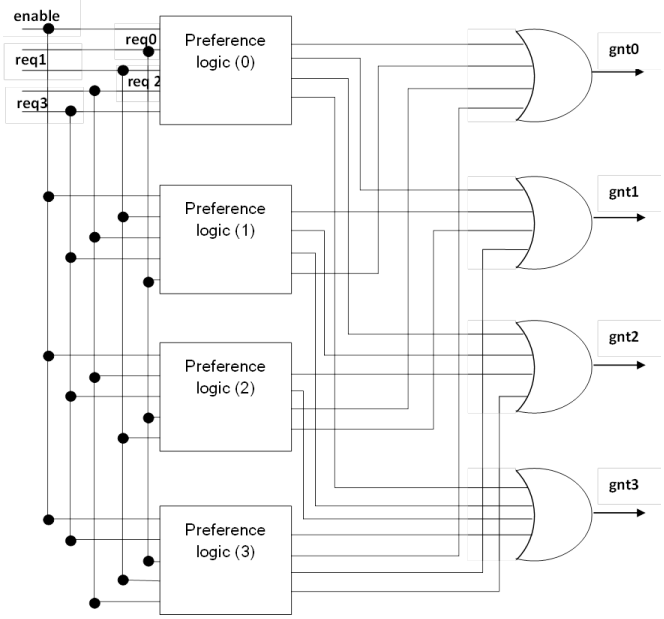


Figure 3: Functional circuit of an arbitor

Behavioral description scheme

Behavioral description has been performed by Verilog hardware description language. Below are behavioral descriptions of an arbitrator.

```
//-----------------------------------------------------
// A four level, round-robin arbiter.
//-----------------------------------------------------
module arbiter (
  clk,
  rst,
  req3,
  req2,
  req1,
  req0,
  gnt3,
  gnt2,
  gnt1,
  gnt0
);
// --------------Port Declaration----------------------
input       clk;
input       rst;
input       req3;
input       req2;
input       req1;
input       req0;
output      gnt3;
output      gnt2;
output      gnt1;
output      gnt0;

//--------------Internal Registers---------------------
wire   [1:0]  gnt     ;
wire          comreq  ;
wire          beg     ;
wire   [1:0]  lgnt    ;
wire          lcomreq ;
reg           lgnt0   ;
reg           lgnt1   ;
reg           lgnt2   ;
reg           lgnt3   ;
reg           lasmask ;
reg           lmask0  ;
reg           lmask1  ;
reg           ledge   ;

//--------------Code Starts Here----------------------
always @ (posedge clk)
if (rst) begin
  lgnt0 <= 0;
  lgnt1 <= 0;
  lgnt2 <= 0;
  lgnt3 <= 0;
end else begin
  lgnt0 <=(~lcomreq & ~lmask1 & ~lmask0 & ~req3 &
~req2 & ~req1 & req0)
       | (~lcomreq & ~lmask1 &  lmask0 & ~req3 &
~req2 &  req0)
       | (~lcomreq &  lmask1 & ~lmask0 & ~req3 &
req0)
       | (~lcomreq &  lmask1 &  lmask0 & req0  )
       | ( lcomreq & lgnt0 );
  lgnt1 <=(~lcomreq & ~lmask1 & ~lmask0 &  req1)
       | (~lcomreq & ~lmask1 &  lmask0 & ~req3 &
~req2 &  req1 & ~req0)
       | (~lcomreq &  lmask1 & ~lmask0 & ~req3 &  req1
& ~req0)
       | (~lcomreq &  lmask1 &  lmask0 &  req1 & ~req0)
       | ( lcomreq &  lgnt1);
  lgnt2 <=(~lcomreq & ~lmask1 & ~lmask0 &  req2  &
~req1)
       | (~lcomreq & ~lmask1 &  lmask0 &  req2)
       | (~lcomreq &  lmask1 & ~lmask0 & ~req3 &  req2
& ~req1 & ~req0)
```

```
      | (~lcomreq &  lmask1 &  lmask0 &  req2 & ~req1
& ~req0)
      | ( lcomreq &  lgnt2);
  lgnt3 <=(~lcomreq & ~lmask1 & ~lmask0 & req3  &
~req2 & ~req1)
      | (~lcomreq & ~lmask1 &  lmask0 & req3  &
~req2)
      | (~lcomreq &  lmask1 & ~lmask0 & req3)
      | (~lcomreq &  lmask1 &  lmask0 & req3  & ~req2
& ~req1 & ~req0)
      | ( lcomreq & lgnt3);
end

//-----------------------------------------------------
// lasmask state machine.
//-----------------------------------------------------
assign beg = (req3 | req2 | req1 | req0) & ~lcomreq;
always @ (posedge clk)
begin
  lasmask <= (beg & ~ledge & ~lasmask);
  ledge   <= (beg & ~ledge &  lasmask)
        |  (beg &  ledge & ~lasmask);
end


encoder encoder (
                  .lgnt0(lgnt0), .lgnt1(lgnt1),
.lgnt2(lgnt2), .lgnt3(lgnt3),
                  .req0(req0), .req1(req1), .req2(req2),
.req3(req3),
                  .lgnt(lgnt), .lcomreq(lcomreq)
                  );
//-----------------------------------------------------
// lmask register.
//-----------------------------------------------------
always @ (posedge clk )
if( rst ) begin
  lmask1 <= 0;
  lmask0 <= 0;
end else if(lasmask) begin
  lmask1 <= lgnt[1];
  lmask0 <= lgnt[0];
end else begin
  lmask1 <= lmask1;
  lmask0 <= lmask0;
end

assign comreq = lcomreq;
assign gnt    = lgnt;
//-----------------------------------------------------
// Drive the outputs
//-----------------------------------------------------
assign gnt3   = lgnt3;
assign gnt2   = lgnt2;
assign gnt1   = lgnt1;
assign gnt0   = lgnt0;
endmodule
```

Below is the behavioral description of preference encoder, used in the arbitrator.

```
module encoder
(lgnt0,lgnt1,lgnt2,lgnt3,req0,req1,req2,req3,
lcomreq, lgnt);
input         req3;
input         req2;
input         req1;
input         req0;
input         lgnt0    ;
input         lgnt1    ;
input         lgnt2    ;
input         lgnt3    ;
output                    lcomreq;
output  [1:0] lgnt;
//-----------------------------------------------------
// comreq logic.
//-----------------------------------------------------
assign lcomreq = ( req3 & lgnt3 )
               | ( req2 & lgnt2 )
               | ( req1 & lgnt1 )
               | ( req0 & lgnt0 );

//-----------------------------------------------------
// Encoder logic.
//-----------------------------------------------------
assign  lgnt =  {(lgnt3 | lgnt2),(lgnt3 | lgnt1)};

endmodule
```

Circuit simulation has been implemented by means of VCS tool. Figure 4 presents the diagrams of the obtained signals.

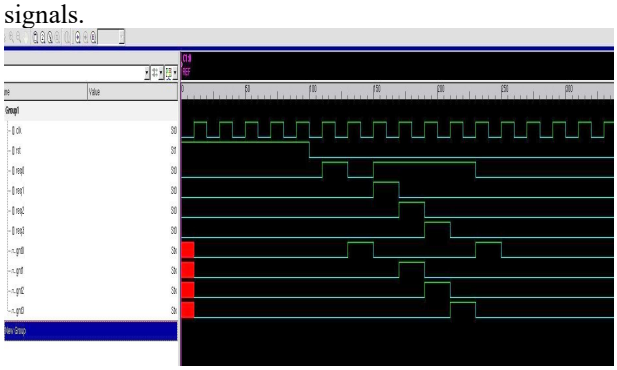


Figure 4: Signals diagram of an arbiter

Statistical static timing analysis of the circuit

The circuit has been synthesized by all contemporary low power design methods. All the circuits have been synthesized by SAED32 nm technology library, which enables the use of all low power design methods. As the

main operating power supply for all circuits, 0,95V was chosen. The same space limit of 150μm^2 has been set for all circuits, which allowed to examine the circuits the same way in terms of the surface. Synchro signal frequency was chosen 50MHz.
By means of statistical static timing analysis method, the total statistical delay of elements from req0 input to gnt0 output has been computed for all circuits.
Below are all the applied methods and obtained circuits, static and dynamic power consumption and the total statistical delay of elements from req0 input to gnt0 output has been computed for all circuits.

Circuit Synthesis by Classical Method
In this case the Design Compiler synthesis tool was given the characterized library for 0,95V.

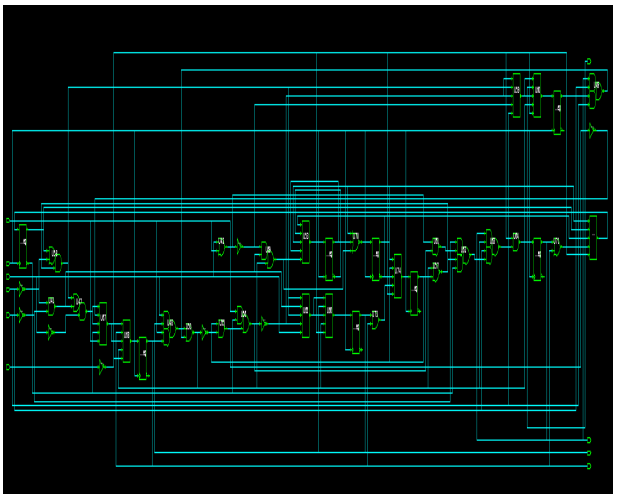


Figure 5: Synthesized circuit of an arbiter by classical method

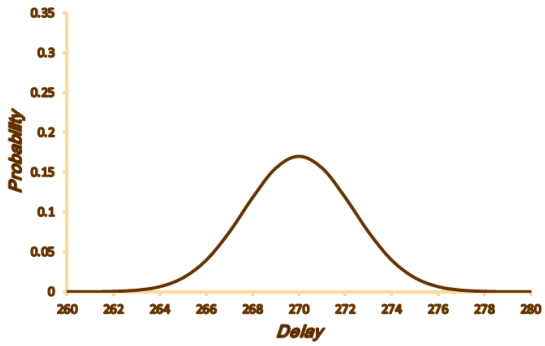


Figure 6: Statistical delay of an arbiter from req0 input to gnt0 output in case of classical method

In this case the circuit consumes 32,3μW power, average value of statistical delay from req0 input to gnt0 output is 270ps, and the standard deviation is 2,345ps.

By scaling of circuit synthesis voltage
In this case, voltage scaling has been implemented, i.e. Design Compiler synthesis tool was given the characterized library for 0,7V.

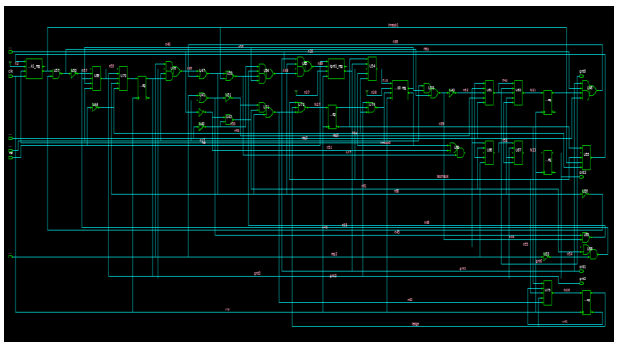


Figure 7: Synthesized circuit of an arbiter by voltage scaling

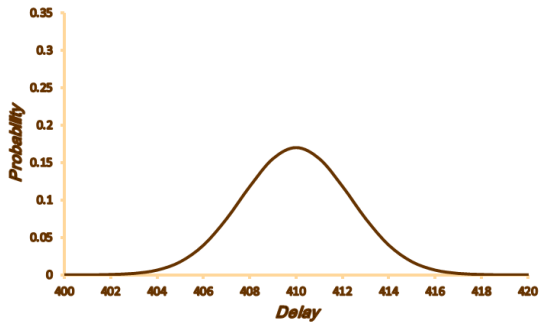


Figure 8: Statistical delay of an arbiter from req0 input to gnt0 output in case of voltage scaling method

In this case the circuit consumes 13.4μW power, average value of statistical delay from req0 input to gnt0 output is 410ps, and the standard deviation is 2.3ps.

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Exploring Second Order s-to-z Transformation for IIR Linear Phase Filters Design

Dejan Mirković, Miona Andrejević Stošović and Vančo Litovski

Abstract – This paper explores design of IIR filters with linear phase exploiting a new second order s-to-z domain mapping. Capabilities of the mapping are exemplified with eight order s-domain filter designed to have constant pass-band group delay and all kind of zeros. New mapping will be confronted with bilinear and phase-invariance method. Results of the numerical analysis showed solid behaviour of new mapping over various sampling rates.

Keywords – IIR Filters, Linear Phase, S-to-z mapping.

I. Introduction

With rapid development of integrated circuit (IC) industry, digital signal processing becomes leading concept of signal conditioning in contemporary circuits and systems. Two key stone concepts of the DSP paradigm are: finite impulse response (FIR) and infinite impulse response (IIR). Both concepts are very important and the first step one should take when designing DSP system is to properly decide which one to apply according to given application. Since linear phase is desired characteristic of the system it is natural to embrace FIR concept only since there is no recursion and linear phase is always possible by design. However, this property is usually paid with higher latency and order (more hardware). On the other side there is IIR concept which can provide same functionality with significantly lower order and latency which makes it attractive for low power design. Unfortunately, IIR concept suffers from poor control over phase characteristics. Therefore, additional circuitry is usually introduced (so-called phase correctors) to mitigate this problem [1].

This paper explores possibility of designing linear phase IIR filters utilizing second order transformation function which tries to simultaneously preserve both magnitude and phase characteristics.

Paper is organized as follows. In the second section methods for designing IIR filters will be briefly discussed. Here second order transformation function, and Phase Invariance Method will be presented. Third section will present results of the numeric analysis. Important findings concerning system stability and usefulness of the second order transformation for IIR filter design will be outlined in the conclusion.

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II. Methods for IIR filters design

The number of techniques and methods for designing IIR filters are derived through endeavour of research community along the past decades. When designing the IIR filter one first must design space i.e. domain. Traditionally design of IIR filters starts form *s*-domain, thus two groups of methods can be identified. One group consists of methods with special purpose. The goal of these methods is to preserve, as well as possible, one particular characteristic of the filter at the cost of the others. In this group one can classify Impulse/Step Response Invariant Method [2, 3] and Magnitude/Phase Invariance Method [4, 5]. Another group of methods is based on substitution of complex frequency s with corresponding expression in z. These methods are usually referred as mapping methods or transforms, e.g. Matched-z [6], Forward/Backward Euler and Trapezoidal (Bilinear) transform [7].

Finally, one may choose to do the design directly in z-domain. Here designer is usually unlikely to find closed form solutions. Most of the design work is done through recursive numerical routines. One comprehensive set of algorithms and routines supporting this approach can be found in [8].

In this work we focus on the methods which belong to the traditional IIR design approach, i.e. transforming analogue *s*-domain filter prototype into *z*-domain.

A. Second order s-to-z transformation

The second order transfer function is introduced by the authors of [9] for the first time. Authors showed that differentiation function in *s*-domain (i.e. simple multiplication with *s*) can be approximated in closed form in *z*-domain with Eq. (1).

$$s = \frac{1}{2T_s}\frac{3z^2 - 4z + 1}{z^2} \tag{1}$$

Here, T_s is sampling period. Observing Eq. (1) one may note that dividing numerator with the denominator second order polynomial in terms of z^{-1} (delay elements) emerges. Therefore, there is no rational function like in *bilinear* case given in Eq. (2), hence expected positive impact on the phase characteristic. Of course, this is paid with twice higher order of the resulting filter in the *z*-domain comparing to mapping with *bilinear* transform.

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{2}$$

Since second order, this new transformation function will be further referred to as *quadratic*. Authors of [9] also proved that *quadratic* transformation preserves stability over wide range of sampling rates, equally well as famous *bilinear* transform. It should be noted that *quadratic* transform belongs to the second group of methods at the beginning of the section. In other words it does not favour any characteristics over the others. On contrary, it tries to preserve simultaneously both phase and the magnitude.

It is also important to emphasise that for proper calculation of the frequency response, and group delay real, analogue, angular frequency ω first must be pre-wrapped i.e. mapped in corresponding digital frequency ω_d. This is done by replacing complex frequency s with $j\omega$ and complex variable z with $e^{j\omega_d}$ in Eq. (1) and (2). In a case of *bilinear* transform this relation is already known and derivation easily performed resulting with Eq. (3).

$$\omega_d = 2\tan^{-1}\left(\frac{\omega T_s}{2}\right) \tag{3}$$

Similar is obtained, involving little bit more effort, for *quadratic*. Derivation of this relation is out of the scope of this paper nevertheless it is given in Eq. (4) for completeness.

$$\omega_d = \tan^{-1}\left(\frac{\sqrt{\sqrt{1+2\omega T_s}-1}}{2\sqrt{2}-\sqrt{\sqrt{1+2\omega T_s}+1}}\right) \tag{4}$$

This way each real frequency is properly mapped in z-domain.

B. Phase-Invariance Method

In order to better examine properties of the *quadratic* transform, method from the second group (special purpose methods) will be utilized as well. This way *quadratic* transform will be confronted with most popular representatives from both, first and second group of methods for designing IIR filters. Since linear phase is target parameter to preserve, Phase Invariance Method (PIM) introduced by Paarmann [5] will be exploited.

Phase invariance is based on Hilbert transforms where magnitude response can be obtained from phase response and vice versa [10]. Transformation algorithm is of algorithmic type where samples of the desired, analogue prototype, phase response given in Eq. (5) are taken as the input.

$$\Phi[k] = \Phi(\Omega),\ \omega = \frac{k\pi}{N},\ k = 0,\ldots,N-1 \tag{5}$$

Algorithm may be fine tuned by proper choosing number of samples N. Since inverse Fast Fourier Fourier (FFT) transform is used, N should be in power of two. This method will further be referred to as *Paarmann*.

In this case there is no closed form relation between complex s and z. Variables frequency response is simply calculated in, $\omega_d = \omega T_s$ points.

III. Results of the Numerical Analysis

For obtaining results and presenting the data, package for numerical analysis MATLAB is exploited. Package already includes almost any possible standard algorithm and routine tools for filter design in *Signal Processing Toolbox*. These are usually readily available in a form of functions. However, non-standard algorithms such as *quadratic* and *Paarmann*, have to be coded. Therefore, custom function is written implementing *quadratic* transformations, while for *Paarmann* transformation implementation given in [11] is used.

As the test case example is rather complicated, eight order filter with approximately linear pass-band phase response is chosen as an example. Selectivity of the filter is improved with introducing zeros (two pairs of purely imaginary and one pair of right hand side – RHS) like described in [12]. Location of the poles and zeros of the s-domain prototypes is shown in Fig. 1.

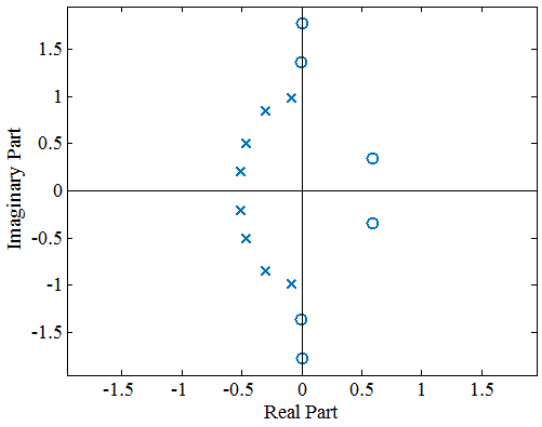
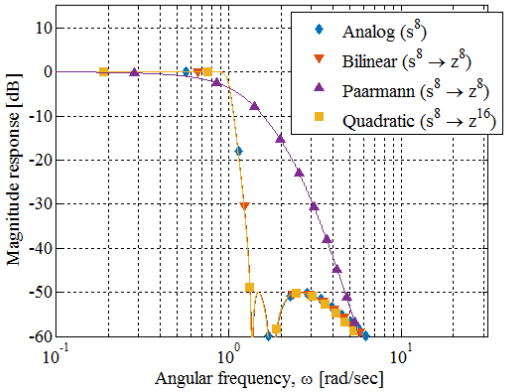
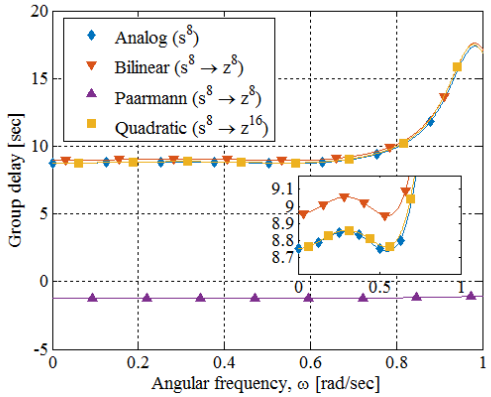


Fig. 1 Poles and zeros location in the s-plane for eight order filter used as test case example.

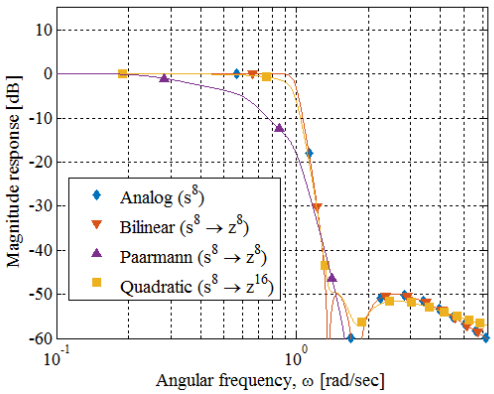
Fig. 2 shows the results of the numerical analysis for various sampling rates. New, *quadratic*, transformation is compared with *bilinear* and *Paarmann* PIM method. Magnitude response and pass-band group delay are evaluated for three characteristic sampling periods T_s ={0.1, 0.5, 2} sec. Starting, analogue prototype filter characteristics are plotted along with digital counterparts.



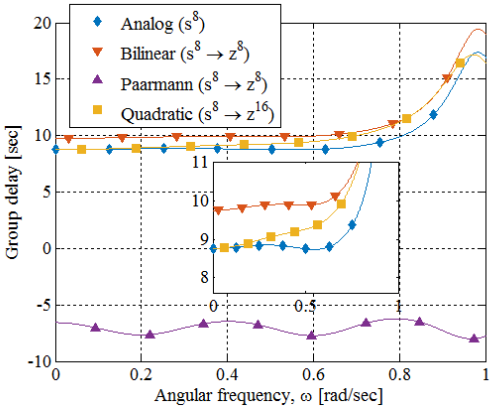
a1) Magnitude response for $T_s = 0.1$sec



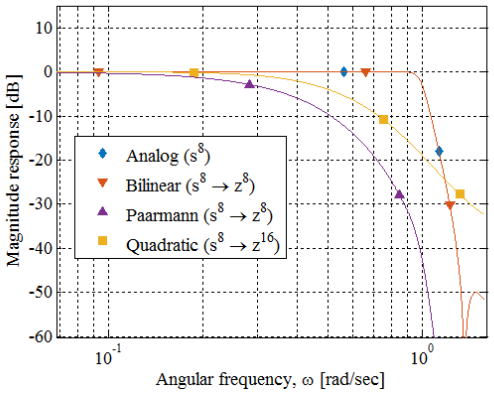
a2) Pass-band group delay for $T_s = 0.1$sec



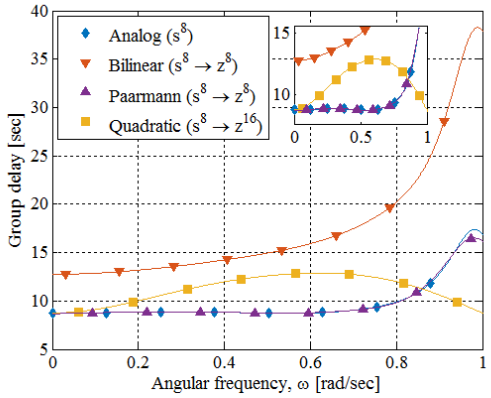
b1) Magnitude response for $T_s = 0.5$sec



b2) Pass-band group delay for $T_s = 0.5$sec



c1) Magnitude response for $T_s = 2$sec



c2) Pass-band group delay for $T_s = 2$sec

Fig. 2 Results of the numerical analysis:
a1), b1) and c1) Magnitude response, and a2), b2) and c2) Group delay for T_s= 0.1, 0.5 and 2 sec, respectively.

All plots are shown to $f_s/2$ since in z-domain everything is periodic with period of T_s.

First test case is for relatively high sampling rate T_s = 0.1 sec (i.e. f_s = 10Hz). Here, *quadratic* and *bilinear* perform well in both, magnitude and phase response. In this case *Paarmann* fails to follow magnitude since it is designed for approximating phase at the expense of the magnitude. Even though it gives constant group delay it does not approximate analogue prototype group delay in value. This is shown in Fig. 2 a1) and a2). However, if zoomed detail in Fig. 2 a2) is observed slight improvement in group delay over *bilinear* is visible when using

quadratic mapping. Next, system is sampled with moderate sampling rate (T_s = 0.5 sec). This is depicted in Fig. 2 b1) and b2). In this case *bilinear* still performs well when magnitude response is observed, while *quadratic* starts to deviate from analogue prototype (Fig. 2 b1)). When looking at group delay *quadratic* again outperforms *bilinear* (Fig. 2. b2)).

Finally, when system is sampled with extremely low rate (T_s = 2sec) *Paarmann* PIM method is the best choice when magnitude response is not of primary concern. Interestingly, *quadratic* gives if not constant than at least smaller group delay comparing with *bilinear*.

To check stability of the system obtained using *quadratic* transformation zeros and poles location is shown in Fig. 3 for extreme sampling rate of T_s = 2 sec.

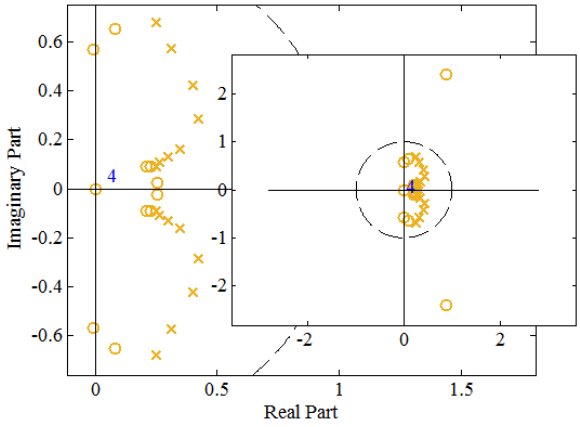


Fig. 3 Zeros and poles location for the *quadratic* transformation for extreme sampling rate T_s = 2sec. Zoomed detail with pole location, behind, and whole picture with two RHS zeros, in-front.

It can be seen that even in this extreme case stability is preserved (all poles inside unit circle). One can note that there are sixteen poles and zeros in the *z*-domain which is direct consequence of second order nature of the transformation.

III. Conclusion

In this paper second order *s*-to-*z* transformation (mapping) is explored for the IIR filter design. First, basic concepts regarding IIR filter design are covered with emphasis on three methods. Two of them are already known to science and engineering community namely, well established *bilinear* and relatively new PIM. The third one, *quadratic*, is introduced by the authors and proved to be usable in the design of IIR filters exhibiting linear phase. Generally, *quadratic* transformation showed a solid behaviour over various sampling rates, while simultaneously trying to preserve both magnitude and phase response of the filter. Robustness of the *quadratic* transformation is confirmed with maintaining filter's stability even under slow sampling rate conditions. Good performance is paid with doubling *z*-domain filter.

Acknowledgement

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CMAC and Chebyshev Filters in Frequency Domain

Dragan Topisirović, Miona Andrejević Stošović, and Vančo Litovski

Abstract - In this paper we will compare the frequency domain behavior of the basic classes of polynomial low-pass filters with critical monotonic amplitude characteristics (CMAC), and Chebyshev filters. We will present phase and group delay characteristics of these filters, and also phase correctors' configurations that will be used to improve these characteristics, i.e. to reduce distortions of group delay. Conclusions as to which solution is preferable in a proper situation will be offered.

Keywords – CMAC filters, Chebyshev filter, frequency characteristics.

I. Introduction

In the available literature, there have not existed systematical comparisons of CMAC filters and their analogue with non-monotonic amplitude characteristic, known as Chebyshev filter [1]. If we want to compare them properly, we need to do that from several aspects: first, from the selectivity point of view; then, we can study their frequency domain characteristics, such as amplitude, phase, group delay, and finally, we can study their time domain characteristics. So, after these analyses, we expect to obtain answers to very interesting question: "Which characteristics are better, CMAC or Chebyshev?"

In this paper we will engage ourselves only in frequency characteristics of the basic classes of polynomial low-pass filters with critical monotonic amplitude characteristics, here referred to as CMAC, and Chebyshev filters.

Critical monotonic functions have the property that the amplitude characteristic in the pass-band has monotonic character with maximal number of inflection points. Also, it is need that amplitude characteristic has maximal number of inflexion points, with different abscissae. In that way, the first derivative of amplitude characteristic is equal to zero for maximum number of times, without changing its sign, meaning that its value is limited, and the sensitivity of the amplitude characteristic to changes of circuit parameters is reduced.

This is applied to four basic classes of CMAC filters [2]:

1. Maximally flat in the origin. This means all derivatives of $L_n(\omega^2)$ at the origin are to be zero.

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The class of filters thus obtained is called Butterworth`s after the author [2]. These will be here referred to as B-filters.

2. Maximum slope of the characteristic function at the edge of the pass-band. The class of filters so obtained is called L-filters and was introduced by Papoulis [4], [5]. The name L comes from the fact that in the original derivation Legendre polynomials were used. In some references [6] it is stated as "optimal filters" which is arbitrary.

3. Maximum asymptotic attenuation. This means the higher order coefficient in $L_n(\omega^2)$ has to be maximal. This class of filters was introduced by Halpern [7]. These will be here referred to as H-filters.

4. Least-squares-monotonic. In this case the returned power in the pass-band was minimized under the critical monotonicity criterion. This class was introduced by Raković and Litovski [8] and named LSM filters.

The paper is structured as follows: In the second chapter we will first give attenuation characteristics of both CMAC and Chebyshev filters, and then phase and group delay characteristics. In order to correct nonlinearities in the group delay characteristics, phase corrector structures are proposed in the third chapter. Finally, conclusions are given.

II. CMAC and Chebyshev Filter Characteristics

The main contribution of this paper is to present for the first time phase and group delay characteristics of CMAC filters.

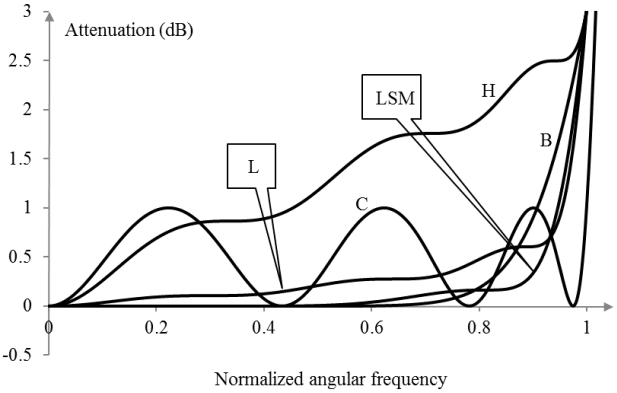


Figure 1. Attenuation characteristics of 7th order CMAC filters, and attenuation characteristics of Chebyshev filter with 1dB attenuation in the pass-band

In order to properly estimate these characteristics, we will also analyze Chebyshev filter with 1dB attenuation in the pass-band, what is average attenuation value of CMAC filters. We will consider here only 7th order filters.

If we analyse both filter types, aiming to compare these characteristics and to decide what filter to choose (or what approximation function to choose), we must consider several filter characteristics that participate in this choice, such as: time domain characteristics, sensitivity to the change of parameter values, what will not be considered in this paper, but in some of our future papers.

First, we will induce some definitions in order to present how frequency characteristics of the mentioned filters are obtained.

Attenuation characteristics of CMAC filters of 7th order, as well as Chebyshev characteristics are presented in Fig. 1. We can notice that Chebyshev filter, as it is defined, has 1dB attenuation at cut-off frequency, but other filters have 3dB attenuation.

However, in the pass-band, Chebyshev filter has larger attenuation at lower frequencies, what can be a disadvantage in the situations when the power density of the signal spectrum is larger at the lower frequencies (e. g. voice transmission). In such situations one needs to use either CMAC or Chebyshev filters with considerably lower attenuation in the pass-band, what causes a considerable reduction of selectivity, leading to increase of filter order for the sake of preserving selectivity.

Attenuation in the stop-band of the mentioned filters is presented in Figure 2. We can notice that from the selectivity point of view, Chebyshev filter dominates.

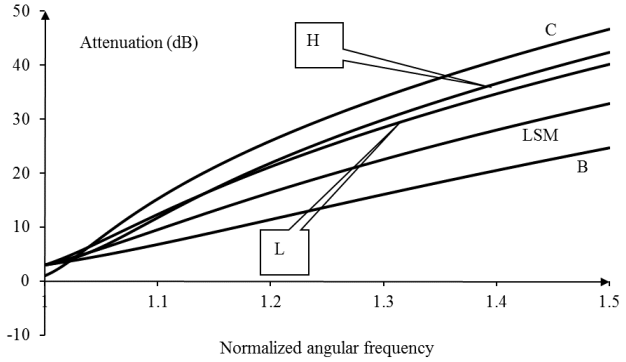


Figure 2. Attenuation characteristics of CMAC and Chebyshev filters in the stop-band

Phase characteristics of the above-mentioned filters are presented for the first time in Figure 3. It is known, but we can also see, that from the graphical presentation of the phase characteristic we can hardly conclude anything about phase distortions, so we usually use group delay characteristics.

They are presented in Figure 4. It is very noticeable here that Chebyshev filter exhibits large distortions of group delay, and also, that group delay is the least distorted by LSM and Butterworth filter.

III. Phase Correctors for LSM and Chebyshev Filters

By observing the group delay characteristics of the filters, we can deliver conclusions about phase corrector complexity that could be eventually used to correct phase delay characteristic, and also, about overall complexity of the cascade- filter+corrector.

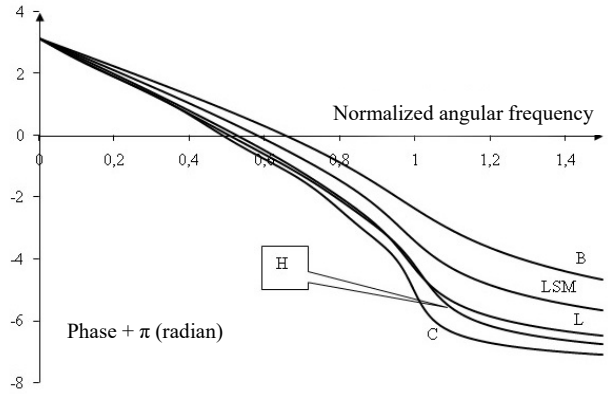


Figure 3. Phase characteristics of the 7th order CMAC and Chebyshev filters

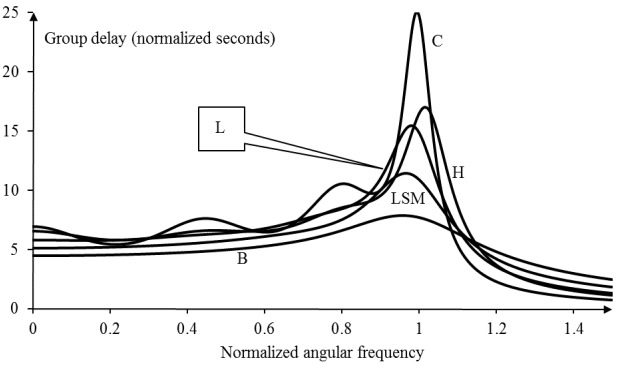
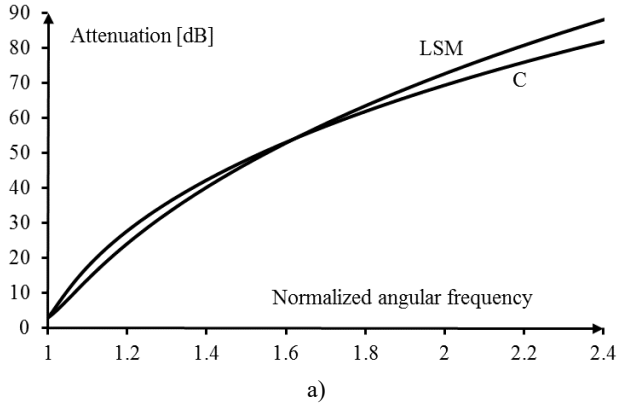


Figure 4. Group delay characteristics of CMAC and Chebyshev filters

As an example in this paper, we will use pair LSM-C (Chebyshev). From the filter theory, we can calculate the value of the highest coefficient in the square of the polynomial in the denominator of the amplitude characteristics of the 7th order Chebyshev filter with 1dB attenuation, and it is $(a_{2n}=a_{14})_{\text{Chebyshev}}=1060.56$. It represents the rate of asymptotic attenuation of the filter, i.e. its selectivity by Halpern criterion. Accordingly, asymptotic attenuation of this filter will be determined by $1060.56\cdot\omega^{14}$. LSM filter of the 9th order, whose highest order coefficient is $(a_{2n}=a_{18})_{\text{LSM}}=154.68$, has almost the same selectivity, so that asymptotic attenuation is determined by $154.68\cdot\omega^{18}$. Amplitude characteristics of these filters are shown in Figure 5, where we can see that

we chose LSM filter with better attenuation characteristics in the pass-band, and almost the same in the stop-band.

If we realize these filters as passive ladder structures, this LSM filter would have two elements more (one inductor and one capacitor).



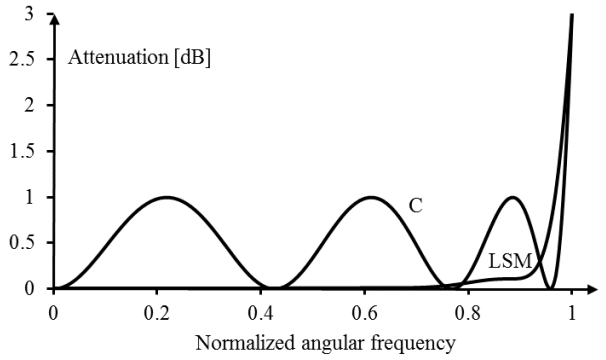


Figure 5. a) Attenuation in the stop-band and b) Attenuation in the pass-band of 7th order Chebyshev filter (1 dB, renormalized) and of 9th order LSM filter

If we design, for the two above-mentioned filters, phase correctors that should lead to small group delay error in greater part of the pass-band, considering the literature ([9], [10], [11]), we can expect that Chebyshev filter requires phase corrector whose order is for 2 higher than LSM filter corrector order (the optimum case-for Chebyshev). In the passive realization, considering complex zeroes, corrector cell has at least 5 elements, thereby using at least one transformer [12]. If we consider active cascade RC realization, extension of LSM filter would be achieved using 3rd order cell (Sallen-Key, for example), that realizes only zeroes in the infinity, but the extension of Chebyshev filter would require complex cell with noticeably greater number of elements (Tow-Thomas, for example).

As an illustration of this claim, we will consider complex filters obtained by cascade of the filter (CMAC or Chebyshev) and phase corrector. In order to obtain a fair comparison, we will use 9th order LSM filter and 7th order Chebyshev filter that is renormalized so that its amplitude characteristics achieves 3dB at cut-off frequency. This can be seen in Figure 1.

Comparison given in this paper is the first of that kind, and it could not be found in existing literature. This includes also the following examples.

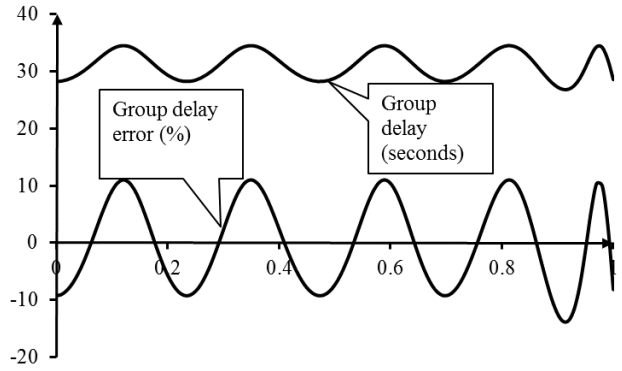


Figure 6. 7th order Chebyshev filter with 8th order corrector. Group delay (up) and error in approximation of constant group delay (down)

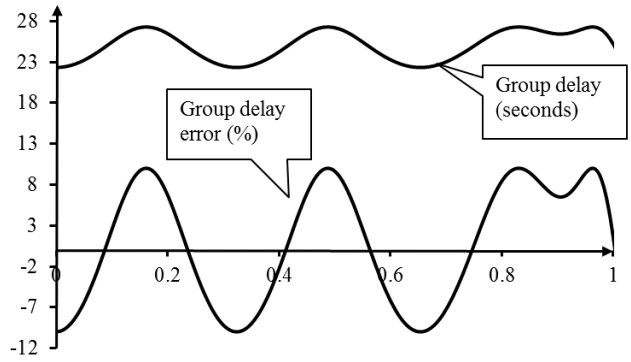


Figure 7. 9th order LSM filter with 6th order corrector. Group delay (up) and error in approximation of constant group delay (down)

If it is required that group delay is constant in the entire pass-band with 10% relative error, we obtain filters with characteristics presented in Figs. 6 and 7. Group delays and corresponding relative deviations are presented in these figures.

In Figure 6 these data are given for 7th order Chebyshev filter. In order to obtain approximation of constant group delay in the entire pass-band with 10% relative error, we needed 8th order corrector. According to theory, in ideal case, the value of group delay in pass-band should be: $\pi\cdot(n+2\cdot k)/2= \pi\cdot(7+2\cdot 8)/2=36$ s.

Here, n is order of the filter, k is order of the corrector. The value $(\tau_{d_mean})_{Chebyshev}=31.28$s, obtained by approximation is less because the part of the area under the group delay curve outspreads outside the pass-band. We should

have in mind that with this corrector complexity, we cannot obtain group delay approximation in the entire pass-band, but this result is accepted as satisfactory.

Figure 7 represents group delay and relative deviations of the corrected 9th order LSM filter. In order to obtain approximation of constant group delay in the entire pass-band with 10% relative error, we needed 6th order corrector. This approximation is a bit better than the one in the Figure 6, but that is not of the big importance. Mean value of group delay of this combination is less than in the case of Chebyshev filter, and it is $(\tau_{d\_mean})_{LSM}$=24.77s. So, we conclude that the combination LSM filter+corrector would have smaller delay (in this case 21%) than the combination Chebyshev filter+corrector (that was reference when calculating relative deviation). Also, it is obvious that the condition that error of the group delay is smaller or equal 10% is easily fulfilled.

So, we can consider that in this way we obtained two filters with approximately same selectivity and approximately same group delay, but the corrected LSM filter exhibits less amplitude distortion in the pass band and smaller delay.

IV. Conclusion

In this paper we presented phase and group delay characteristics of CMAC filters for the first time. We used also Chebyshev filters frequency characteristics as a referent example for comparison.

We used pair the LSM- Chebyshev filter in the filter+corrector cascade to explore which combination would give better results, so we concluded that filters had almost the same selectivity, but the corrected LSM filter exhibited smaller delay and less amplitude distortion in the pass band.

Acknowledgement

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Class-D Audio Amplifier using Pulse Width Modulation

Jovan Galić, Tatjana Pešić-Brđanin, Lejla Iriškić

Abstract - In this paper, a class-D audio amplifier uses MOSFETs in switching mode is designed. The whole system, in addition to amplifiers, contains a pulse width modulator and an output low-pass filter. Either pulse width modulation signal or pulse density modulation signal can be used to drive class-D amplifier stage, and in this paper both techniques are used. The entire system is simulated in PSpice. It is shown that the total harmonic distortion of class-D amplifier is highly influenced by the switching frequency.

Keywords – Class-D audio amplifier, Pulse width modulation, Pulse density modulation.

I. Introduction

Analog power amplifiers have been used for a long time in audio technique [1,2]. There are three classes of audio amplifiers (A, B and AB) which also names as linear power amplifiers. The basic characteristics of linear power amplifier are slightly signal distortion and low power efficiency. The power efficiency of linear amplifier is 30–40% practically in spite of 78.5% theoretically. It, for the desired output power level, means more chip area and additional cooler to reduce heating [2,3].

Class-D power amplifier operates in a switched mode, has high power efficiency and it is able to be digitalized. These characteristics give class-D amplifier significant advantages in many applications because the lower power dissipation produces less heat, saves circuit board space and cost, and extends battery life in battery-powered mobile systems [3,4]. Therefore, class-D amplifiers are becoming preferred in consumer electronic products such as DVD, LCD-TV, MP4, cell phone, hearing instruments, wireless headsets, computer multimedia, etc [2-5].

The modulation techniques commonly applied for the realization of analog/digital class-D amplifiers are either pulse width modulation (PWM) or pulse density modulation (PDM). The choice of modulation techniques (and the parameters of the selected technique) affects the sound quality at the amplifier output. In this paper, we analyze the impact of switching frequency on harmonic distortion of output signal for both techniques of modulation.

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II. Class-D Amplifier Architecture

The class-D amplifier differs from other conventional amplifier classes because it works on a completely different principle. This type of amplifier is called the "digital" amplifier, because of the shape of the output signal, although the digital amplifiers are considered circuits that enhance the digital signals. The operation of the class-D amplifiers is based on pulse width modulation, so a typical class-D amplifier contains a modulator.

The modulator converts an audio signal (analog or digital) into a stream of pulses. The pulse widths depend on the amplitude of the audio signal, while the spectrum contains an audio signal and unwanted high-frequency components. This modulated signal drives the output stage, often a half- or full-bridge power switch. Switching output stage transistors (MOSFETs) are always fully on or fully off because they are amplifying a two-level signal. In that way, the operation of the MOSFETs in the triode region (where power efficiencies drop) is avoided. When a transistor is on, the voltage across it is ideally zero, while when the transistor is off the current through it is considered to be zero. In any case, the power dissipation of the output level will be equal to zero, which means that the ideal power efficiency of the switch is equal to 100% and can reach greater than 95% power efficiency in practice with appropriate design [6].

After amplification of the modulated signal, the switch output signal contains audio signal and high-frequency components. The output signal must be filtered before it can be sent to a speaker. The last stage is the filter stage , or demodulation stage, which consists of a low-pass filter (LPF). The signals in the audible range (up to 20 kHz) pass through LPF, while the high-frequency signals (above 20 kHz) are significantly attenuated. Filtered analog output signal is an amplified replica of audio analog input signal.

The feedback network from the power stage output to a modulator input (which can be active or passive), suppresses total harmonic distortion produced by power stage non-linearities and non-idealities. The negative feedback control loop also reduces the pulse-height errors [3].

Figure 1 shows block diagram of class-D amplifier (a) and typical architecture of this amplifier (b) [7].

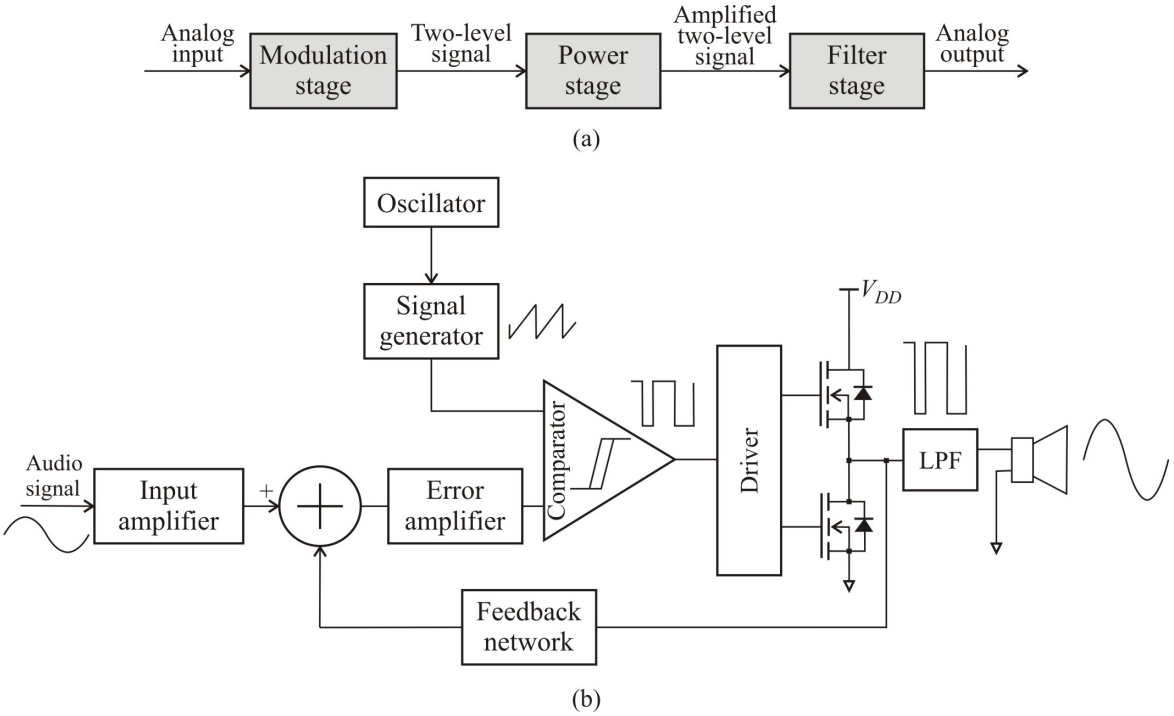

Fig. 1. Block diagram of class-D amplifier (a) and typical architecture of class-D amplifier (b)

III. Modulation Stage

The great significance of the amplifier has a modulation stage. The loss of information in the modulation causes distortion of the audio signal and significant decreases sound quality.

There are many techniques of modulation that can be used in class-D audio amplifier. The choice of modulation techniques is often determined by the requirements that relate to simplicity and effectiveness. A simplified design means a use of smaller number of components and a lighter and more portable device. Effectiveness is important characteristics because modulation is essential to sound quality and the amplifier must achieve less than 1% distortion and greater than 90 dB Signal to Noise Ratio (SNR) [8].

The most commonly used modulation techniques are pulse width modulation (PWM) and pulse density modulation (PDM).

A. Pulse width modulation

The pulse width of PWM modulator output is varying with the amplitude of the input signal. A fundamental system to create pulse-width modulated signals is shown in Fig. 2 [7].

In PWM technique, the input audio signal v_m is compared with the carrier signal v_c. If the input signal is higher than the carrier signal, the output signal v_{PWM} will be set to a higher value (v_H). Otherwise, the output signal will have a lower value (v_L): If the input signal is higher than the reference, the pulse is switched to the high level, otherwise to the low level:

$$v_{PWM}(t) = \begin{cases} v_H & \text{for } v_m(t) > v_c(t), \\ v_L & \text{for } v_m(t) < v_c(t). \end{cases} \quad (1)$$

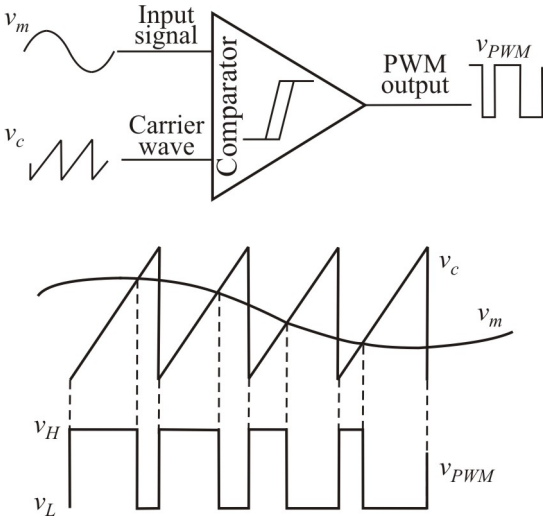

Fig. 2. Fundamental PWM principle

The period of the carrier signal defines the cycle-time of the PWM pulses.

Two important parameters of the PWM modulation can be defined:

- The ratio F of the carrier frequency f_c and the input signal frequency f_m, which defines the spectrum of the PWM output signal. In practical modulators this ratio is higher than the 10.
- The modulation index M, which is the ratio between the input signal amplitude V_m and the amplitude of the carrier signal V_c. Preferably, the $M < 1$ for the PWM modulation.

The main disadvantages of PWM are the inherent nonlinearity of the PWM process which causes the distortions in audio signal baseband in many applications and extremely small pulse width in the case of full modulation.

B. Pulse density modulation

In many applications, PDM can be used instead of PWM. In pulse density modulation, the number of pulses in a time window is directly proportional to the average value of the input audio signal. In PDM technique, width of individual pulses can not be arbitrary, but is instead quantized to multiples of the modulator clock period.

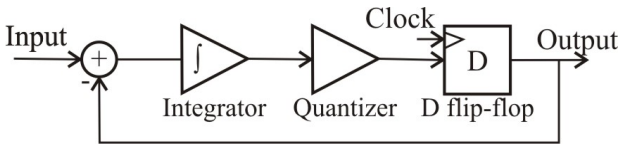

Fig. 3. First-order sigma delta (ΣΔ) modulator

PDM signal conversion can be realized by the analog or digital 1-bit sigma delta modulator (ΣΔ modulator). ΔΣ modulator can be realized using only an integrator and a D latch, as shown in Fig. 3. The audio signal is the input to a integrator circuit. When this signal surpasses a threshold, it resets the integrator and triggers the D-latch. This provides a series of set-width pulses at the output with variable spacing between them, whose time density distribution represents the instantaneous amplitude of the original input signal [7]. To reduce the quantization noise, the switching frequency must be significantly greater than the frequency of the input signal.

Due to the oversampling, the switching frequency can be large, which means higher power dissipation than in case of PWM. On the other side, ΣΔ technique provides better linearity than the PWM technique.

IV. Results and Discussion

In this paper, influence of switching frequency on harmonic distortion of output signal is examined, for both techniques of modulation. Parameter for estimation of distortion is total harmonic distortion (THD), which is defined as:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots}}{V_1} \cdot 100[\%], \qquad (2)$$

In eq. (2), V_n is RMS (Root Mean Square) voltage of respective harmonic (V_1 is RMS of fundamental frequency). Since in practice harmonics higher than fifth do not contribute significantly to THD, we were taken 5 harmonics into consideration.

The PSpice scheme of PWM class-D amplifier with modulation index M=0.95 is depicted in Fig. 4.

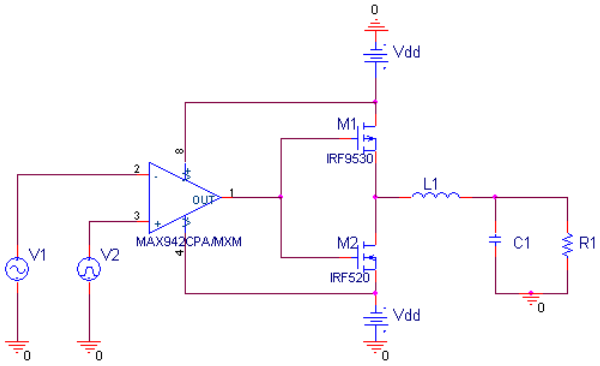

Fig. 4. The PSpice scheme of class-D PWM amplifier

The PSpice scheme of class-D amplifier with one bit sigma-delta modulation is depicted in Fig. 5.

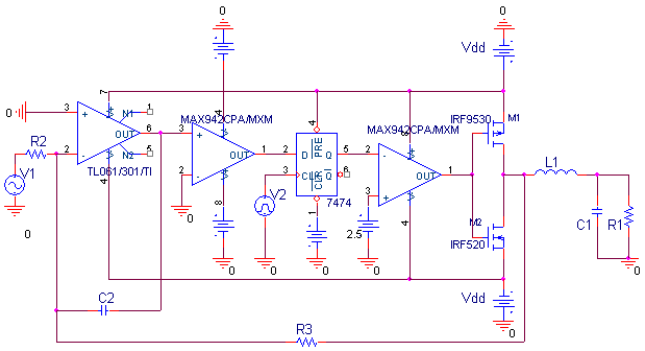

Fig. 5. The PSpice scheme of class-D PDM amplifier

As can be seen from Fig. 5, the PDM amplifier uses one bit sigma delta modulation instead of PWM stage in PWM amplifier. To avoid saturation of integrator stage at the beginning of PDM amplifier, time constant R_2C_2 should be greater than period of pulse generator signal $T_s=1/F_s$ [9]. In this paper, time constant $R_2C_2=2T_s$ has been used. The feedback resistor is with resistance R_3=100 kΩ.

At the output of both techniques, the low-pass passive Butterworth filter of second order with cut-off frequency 18 kHz (L_1=100 μH and C_1=0.68 μF) is used.

As well, supply voltage is ±5 V, and load speaker is approximated as a simple resistance of 8 Ω. MOS transistors (IRF 9530 and IRF 520) are with the on-state resistance 0.2 Ω and maximum current 10 A [10,11]. Speed comparator MAX942 [12], with propagation delay 80 ns

has been used in both the PWM and PDM modulation techniques. As input signals, we used test tones of amplitudes 1 V and frequencies 1 kHz and 5 kHz. For a test tone of 5 kHz, THD calculation was included only components in audio range (i.e. first three harmonics) [7].

The switching frequency is adjustable from 300 kHz up to 800 kHz, with 100 kHz step. A summary of simulation results is presented in Table I.

TABLE I
THD (IN %) FOR PWM AND PDM MODULATION IN DEPENDENCE OF SWITCHING FREQENCY

	Frequency of test tone			
	PWM		PDM	
Frequency [kHz]	1kHz	5kHz	1kHz	5kHz
300	3.06	2.64	1.83	11.53
400	4.76	4.21	0.92	3.46
500	6.42	5.68	0.52	5.79
600	7.46	7.16	0.65	1.07
700	8.77	8.41	0.35	1.01
800	9.94	9.03	0.32	1.49

The above simulation results show that the distortion of output signal is highly affected by the switching frequency.

In PWM modulation, increasing switching frequency contribute to higher THD. In these experiments, for PWM modulation the lowest THD is obtained with switching frequency 300 kHz. The time waveform for 5 kHz test tone and corresponding output signal is depicted in Fig. 6.

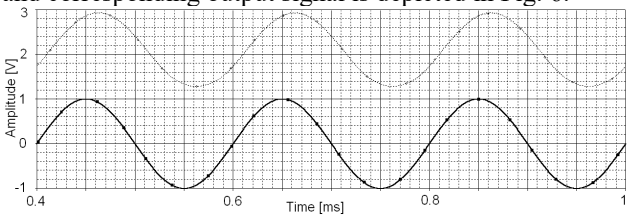

Fig. 6. Time waveform of test tone (solid line) and output signal (dotted line)

In PDM modulation THD is low enough as long as the switching frequency is sufficiently high, where obtained THD is by an order of magnitude lower than for PWM modulation.

It is important to emphasise that the THD value for PDM modulation is highly sensitive to number of quantization bits [13]. Relatively high values of THD is a consequence of conventional, less accurate 1-bit quantization.

IV. CONCLUSION

In this paper we analyzed the influence of switching frequency on total harmonic distortion of the class-D audio amplifier output signal. The analysis was done for two modulation techniques, PWM and PDM. Results of circuit simulations obtained by PSpice show that THD for PDM has a lower value for higher switching frequencies.

Since THD only includes distortion for a single test tone, future work will include tests for intermodulation distortion and analysis of efficiency as well.

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Design of RF power amplifiers at 40.68 MHz

Dušan Petrović, Predrag Petković

Abstract - Paper describes challenges related to the design of RF power amplifier operating at 40.68MHz with high efficiency. The amplifier is aimed to drive a welding actuator in a blood separator device. Therefore the paper begins with brief description of dielectric welding theory and proceeds with explanation of RF generator role in the process. Then the requirements related to welding plastic tubes used for blood separation are defined. The essential part of the paper discusses a design process of RF generator. The main request was to obtain the most efficient solution based on using MOS transistors. Accordingly a design of Class E power amplifier is considered. Finally, simulations and parametric analyses verified a design that provides more than 50W on 50Ω load with efficiency of over 80%.

I. INTRODUCTION

Bodily fluids usually are stored in sealed plastic bags. The bags are filled trough plastic tubes. Therefore it is sufficient to seal the tubes. Special equipment provides reliable watertight closing by welding plastic tubes. These devices utilises the elementary welding theory. The tube has to be heated until begin to melt. Then it has to be exposed to a pressure for a certain amount of time sufficient to seal walls of tube together. As the tubes are made of a dielectric material, plastic, the most efficient way to heat it is to utilize dielectric loses caused by high frequency RF signals. In general this technique is often used in industry when fast and reliable sealing is needed. Depending on particular purpose the power needed for the welding process range from a few tens to several hundred watts [1]. This paper considers an RF generator that should provide output power of at least 50W on 50Ω load. The presented results are extension of previously published paper by the same author [2].

The paper is organized in five sections. The following section describes basic theory of RF sealing. The third section presents a brief description of the main blocks of the device for welding plastic tubes. The central part of the paper describes the design of the crucial part of the welding device – the output amplifier of the RF generator. The chosen solutions are verified by simulations and appropriate analysis in the fifth section. The obtained results proved that the designed solution of Class E amplifier delivers required power of at least 50W to the load with efficiency better than 80 %.

II. RF WELDING THEORY

Temperature is the crucial parameter responsible for melting of any material. At some temperature level interconnecting bonds between particles (atoms, molecules) get lose so that one material turns from solid to liquid phase.

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If two pieces of melted material are pressured, they easily can be mixed making a joint after cooling and returning into solid phase. Besides temperature and pressure the third parameter that controls the welding is time.

The heating phenomenon initiates friction between moving particles. The greater the friction the higher the temperature. Therefore one needs to cause particles movement in order to obtain heat. The moving can be elicited by exposing material to an alternating electrical field. Often change of polarity provoke dipoles to turn from one to another direction causing friction.

According to the AC signal frequency different types of heating are recognized: induction heating, RF or HF heating, microwave heating, infra-red heating. Fig. 1 illustrates the frequency range for each of these types of heating [1].

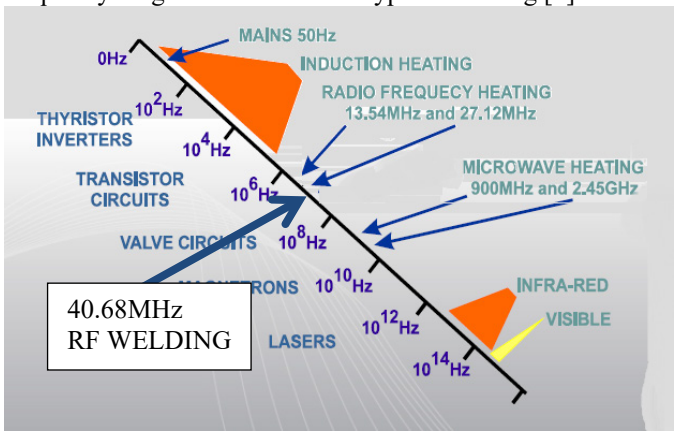

Fig. 1. Frequency ranges that are used for different types of heating materials, reprinted from [1]

Each range has advantages and drawbacks for different applications. The most appropriate frequencies for heating insulators (and poor conductor materials) are RF signals ranged from 1MHz to 200MHz. In order to avoid interfering and disrupting radio communication International Telecommunication Union (ITU) in article 1.15 of Radio Regulations [3] defined ISM RF band for "Operation of equipment or appliances designed to generate and use locally radio frequency energy for industrial, scientific, medical, domestic or similar purposes, excluding applications in the field of telecommunications". In RF band the allowed ISM frequencies are 13.56MHz, 27.12MHz and 40.68MHz. Besides, there are reserved ISM frequencies in microwave band 915MHz, 2450MHz, 5800MHz, and 24.125GHz [3].

In RF electric field dipoles of a dielectric start to alternate direction and due to the friction of molecules within the material it start to heat. It is quite expected that the heating power will be proportional to the frequency. Besides it will be affected by electric field as external factor but also with the

property of the material like dielectric constant and the loses according to the following formula:

$$P = 0.555 * f * E^2 * \varepsilon * (\tan\delta * 10^{-6}). \quad (1)$$

P - heat generated per unit of volume [W/cm^3]
f - frequency of electromagnetic field [MHz]
E – electric field [V/m]
ε - dielectric constant of material [F/m]
tanδ - tangent of the angle of losses [4].

Obviously, the material with higher dielectric constant and higher losses, will heat more. The RF heating can be utilised for welding if the amount of generated heat is sufficient to cause melting of the material. The welding depends on time and pressure, as well. Therefore it is crucial to put the melted material under sufficient pressure for appropriate time to ensure that the melting heat stays in the material until reaching proper sealing.

RF welding technique is commonly used in medicine for sealing plastic materials that keep liquids because it heats containers locally without affecting its valuable contents. Explicitly most of liquids required in hospitals are kept in plastic bags (blood, blood derivate, infusion...). The bags are filled in or out through plastic tubes that should be sealed to preserve a sample of fluid. It is desirable to finish the sealing process for as quickly as possible with minimal impact on its contents.

The following section describes a device for plastic tube sealing that is used in blood donation.

III. PLASTIC TUBE WELDING DEVICE

In general RF welding device consists of:

- Actuator (the welding unit)
- RF generator
- Control logic
- Power supply

Fig. 2 depicts how each of the blocks are interconnected with other.

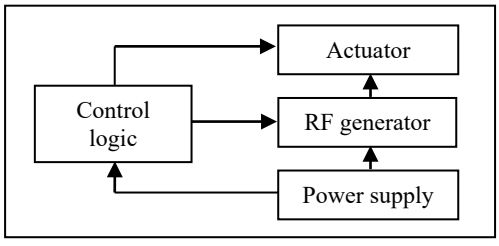

Fig. 1. Block diagram of RF welding device

The welding device that is subject of this paper follows the same structure but has some specifics related to its implementation particular applications.

Actuator is the part where the welding process occurs. The welding material is plastic tube. Therefore it should be settled between two electrodes that provides RF electric field. Practically electrodes with dielectric in between form a capacitor. One electrode is fixed while the other is movable so it can be released and pressed. At the beginning it is released and allows tube to be placed. Then electromagnet presses the movable electrode and RF signal is applied. If the electric field is sufficient, the plastic starts to heat until melting point. As being pressed, it is welded, sealing the tube.

The appropriate electric field is caused by high voltage on the electrodes. The easiest way to produce high voltage on a capacitor is to use serial resonant (LC) that operate at resonant frequency. Therefore an inductor connected in series with the capacitor has to be an integral part of the actuator. Shape of electrodes affects efficiency but this part has solved mechanical engineers. Electrical engineers have to resolve other three blocks.

RF generator provides 40.68 MHz signal that delivers 50W to the actuator. The control logic block manages the process of welding. The RF generator and control logic are powered from DC power supply.

The most challenging part was RF generator and the rest of the paper describes its design.

IV. RF GENERATOR

RF generator has the task to provide signal capable to stimulate the actuator with adequate output power. As previously mentioned the signal should have frequency of 40.68MHz that provides power greater than 50W at 50Ω load. This can not be made in a single stage. Firstly it is necessary to generate 40.68MHz signal in oscillator stage. Then an amplifier is needed to gain amplitude until sufficient electric field is obtained in the actuator. The amplifier is divided in two sections: preamplifier and power amplifier. Preamplifier increases signal from oscillator giving the sufficient strength to excite the power amplifier. Additional requirement is to design output stage as efficient as possible. This constraint comes from the need to supply the device from an external battery.

The load is serial resonant circuit and output is optimised for resonant frequency. Consequently the linearity is not the issue so that class C, D or E amplifiers seem to be good solutions. The design started from the class C power amplifier presented in Fig. 3.

It consists of a pair of transistors Q1 and Q2 connected in push-pull configuration. Both are the same polarity type (npn) transistors and need to be excited with opposite phase signals that come from transformer T1. Transistors are loaded with parallel resonant circuit configured by L1 and C4 in parallel to output capacitance of transistors. Values of L1 and C4 are tuned to the resonant frequency of 40.68MHz. Capacitors C5 and C6 decouples balun transformer T2, made of six composite coils. It balances the differential output impedance of the amplifier to the single ended impedance of the actuator. Serial resonant circuit LA-CA represents actuator model. As capacitor CA form welding electrodes with plastic tube in between, its capacitance is predefined with physical dimensions of electrodes, size of plastic tube and properties of the plastics. Therefore inductance LA is tuned to fit the

resonance frequency of 40.68 MHz with capacitance of electrodes CA. Additional matching between output impedance of the transformer and the actuator utilizes Π filter that consists of L2, C7 and C8.

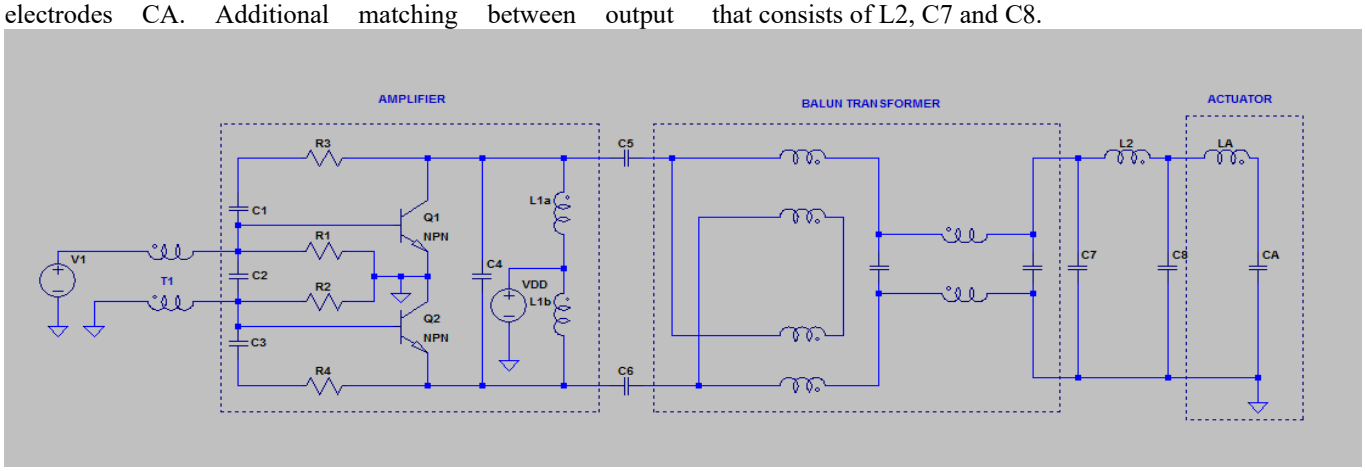

Fig. 3. Electrical scheme of output stage of RF generator

The amplifier in Fig. 3 delivers 50W at 50Ω load but operates with efficiency of less than 70 % when supplied from 15V DC.

Aiming to get better efficiency we decided to design RF generator with output stage operating in class E. The following section describes attempts and realizations achieved.

V. CLASS E RF POWER AMPLIFIER DESIGN

The main source of power dissipation on a transistor is situation when transistor drives considerable current simultaneously with large voltage drop across. Oppositely, when transistor operates as switch dissipation is minimal. Namely, when transistor is turned-off (switch opened) no current flew while the voltage across the switch is maximal – consequently the dissipated power is zero. When the switch is closed (transistor turn-on) it conducts maximal current but voltage drop across is almost zero so the dissipation tends to zero. This theory is built in all energy efficient solutions. Class E amplifiers are one of them [5]-[8]. In an ideal case, efficiency of class E amplifiers is 100%. In practice it can reach up to 96%. Fig. 4 illustrates basic schematics of a class E amplifier realized with an nMOS transistor operating as a switch.

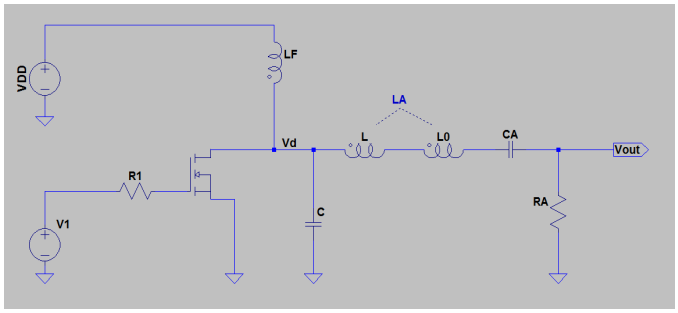

Fig. 4. Class E amplifier

In the switching mode drain voltage changes between VDD and zero trough inductor LF. The drain is loaded with a capacitance C in parallel with serial resonance circuit of the actuator: LA and CA with serial resistivity RA. Practically LA consists of L and L0 (LA=L+L0). During the switching the circuit changes configuration alternating two equivalent circuits for each half of the cycle. When the transistor is on, C is shorted and only LA in series with CA exists. When transistor is off C (togather with parasitic output capacitance of transistor, C_{DS}) is connected to LA and CA. The inductance L has role to match the optimum operating regime. Details about class E amplifiers one can find in [5, 6].

Class E amplifiers are invented and are used to provide the highest possible efficiency (η) by reducing dissipation on transistor. The efficiency represents the ratio of the useful power at the load and the invested power from DC supply. The load power is defined as:

$$P_{OUT} = \frac{1}{2} \cdot \frac{V_{OUT}^{\ 2}}{R_A}, \tag{2}$$

where V_{OUT} denotes amplitude (peak) of the load voltage. The supplied DC power is:

$$P_{DD} = V_{DD} \cdot I_{DD}, \tag{3}$$

where V_{DD} and I_{DD} stands for DC (average) voltage and current, respectively. Consequently, the efficiency is:

$$\eta = \frac{P_{OUT}}{P_{DD}} \cdot 100\%. \tag{4}$$

The difference between useful power at the output and the supplied power is mainly dissipated on transistor. The wasted power depends on the switching speed of transistor and its resistivity while conducting.

On the other hand, the output power depends on RA. However, the values of CA and RA are predefined with the actuator geometry and the properties of plastic tubes that should be sealed. From (1) it is known that the thermal power

will be better for higher frequency, higher field and greater loses. As the frequency is restricted by ITU regulations, and properties of the tube material are predefined, the possibilities of trading for efficiency are very limited. They reflect in selecting fast transistor and in tuning L and C values. In order to meet the design specifications we chose transistor LK701 as active device [9].

Fig. 5 depicts simulation results when the circuit in Fig. 4 is supplied with V_{DD} = 24V and exited from the pulse generator V1 with amplitude of 10V at 40.68MHz. The picture shows waveforms of the output voltage V(Vout) and the drain voltage V(Vd). During simulation the battery provides average (DC) current of 450mA. Consequently, the implementation of equations (2), (3), and (4) responded with the output power P_{OUT} = 9W, the DC supplied power P_{DD} = 10.8W, and efficiency of η = 83%.

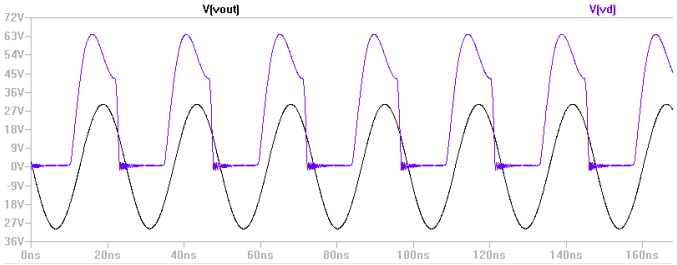

Fig. 5. Simulation results of class E amplifier

Although the efficiency looks acceptable, the main request for the load power is far below the desired specifications. One of possibilities to increase the output voltage (electrostatic field E) is increasing level of power supply. However due to voltage pick caused on LF, when the transistor is turning off, treats to overdrive V_{DS} voltage on drain. Therefore a transformer (L1, L2) is implemented as Fig. 6 illustrates. The transformer firstly the transformer should increase the output voltage. Therefore it has transmission ratio is 1:3. Besides, it helps in matching the impedances of the actuator and the output impedance of transistors. Simulation results of the modified class E amplifier are shown in Fig. 7.

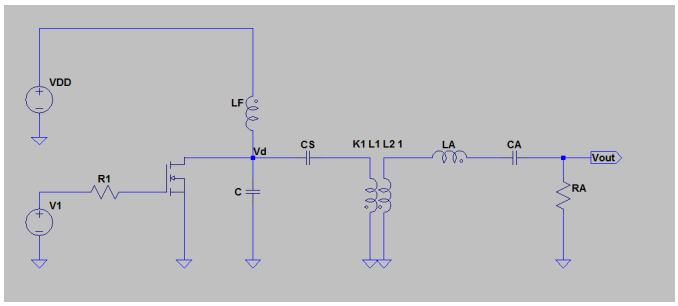

Fig. 6. Modified class E amplifier

This modification increased the output power to P_{OUT} = 45W but DC power raised even more, to P_{OUT} = 45W. Accordingly the efficiency has declined to η = 73%. Actually, the finite transistor output resistance in combination with the parasitic capacitances restrict the transition time when transistor tends to turn on. In order to provide more current to the output, two transistors in parallel were implemented as Fig. 8 illustrates. This modification requires more complex output transformer that consists of L3, L4, L5 and L6. However, L3 and L5 took the role of LF so that the complete circuit complexity is optimized.

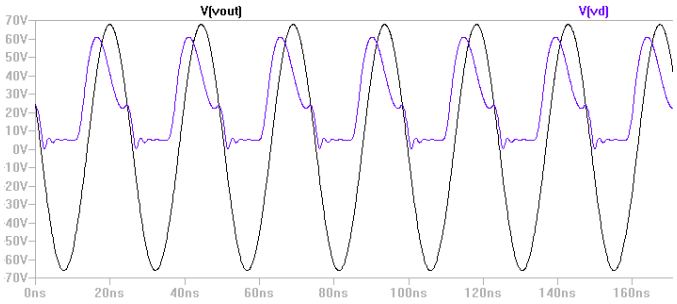

Fig. 7. Simulation results of modified class E amplifier from Fig. 6

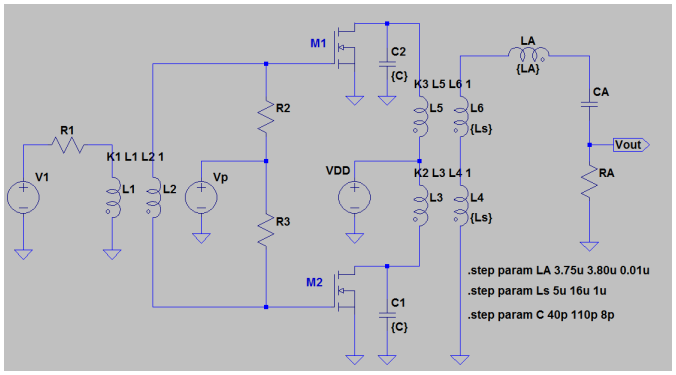

Fig. 8. Class E amplifier after second modification

The transistors operate in anti-phase mode. When one is turned on the other is off and vice versa. This mode provides excitation by transformer (L1, L2). DC voltage threshold voltage was optimized to V_p=4V in order to bias MOS transistors through resistors R2 and R3. The amplifier supply was retained to V_{DD} = 24 V.

The output transformers (L3, L4) and T3 (L5, L6) are designed to sum at the secondary. Therefore they have independent cores with winding direction as shown in Fig. 8. As mentioned above, the values of RA, CA and the frequency of the stimulus V1 are predefined. Consequently, only parameters that could be adjusted for the highest output power are LA, C1, C2 and transmission ratio of the transformer. However, same parameters impact the supplied current so that the higher output power mean better efficiency.

In order to find optimal solution several parametric analyses has been done. For each value we computed output voltage (V_{OUT}), current through the source (I_{DD}), output power, DC supply power (P_{DD}), and the efficiency.

Firstly we considered the effects of capacitances C1 and C2 (denoted as {C}). These capacitances are consisting parts of power amplifier that operates in class E. Their value was swept in range from 40pF to 110pF. The results of the analysis are shown in Table 1. The starting capacitance of 40pF was slightly increased and it can be seen that at some point output voltage starts to decrease which implies decreasing of output power. From Table 1, it is obvious that

acceptable values are between 48pF and 56pF, because only in that range the output power is greater than 50W, which was the starting condition for realization of RF generator. As the higher efficiency (80.43%) was obtained for 56pF, this value was adopted for further analysis.

TABLE I
EFFICIENCY REGARDING C

C [pF]	V_{OUT} [V]	I_{DD} [A]	P_{OUT} [W]	P_{DD} [W]	η [%]
40	70.4	2.71	49.56	65.04	76.20
48	71.0	2.64	50.41	61.36	79.56
56	70.7	2.59	50.00	62.16	80.43
64	70.5	2.57	49.71	61.68	80.60
72	70.0	2.55	49.00	61.20	80.06
80	69	2.53	47.61	60.72	78.41
88	68	2.52	46.24	60.60	76.30
96	67	2.52	44.89	60.60	74.22
104	66	2.51	43.56	60.48	72.16

The second parameter to adjust is transmission ratio of transformers (L3, L4) and (L5, L6). In LTspice this can be done by parametric change of inductances on secondary coil (denoted as {Ls} in Fig. 8). Ls was swept from 5µH to 15µH. Like in the previous analyse, output voltage (V_{OUT}), current through the source (I_{DD}), output power, DC supply power (P_{DD}), and the efficiency were computed for each value of secondary inductance. The results of the analysis are shown in Table 2.

TABLE II
EFFICIENCY REGARDING LS

Ls [uH]	V_{OUT} [V]	I_{DD} [A]	P_{OUT} [W]	P_{DD} [W]	η [%]
5	52	1.55	27.04	37.20	72.68
8	63	2.14	39.69	51.36	77.27
9	67	2.36	44.89	56.64	79.25
10	71	2.59	50.41	62.16	81.09
11	73	2.83	53.29	67.92	78.45
12	76	3.05	57.76	73.20	78.30
15	78	3.70	60.84	88.80	68.51

It can be seen that the rising of transmission ratio increases both the output power (P_{out}) and the current through the power supply (I_{DD}). Design objective of Pout>50W meet all Ls>10µH. However, the maximal efficiency of 81.09% provides Ls=10µH. Consequently this value was adopted for further analysis. It corresponds to transformation ratio of 1:1.41 because the inductance of primary is 5µH.

The third parametric analysis is used to match inductance of LA. Practically there is not much room for it because LA needs to be matched with capacitance of electrodes (CA), in order to make serial resonant circuit. Therefore LA was swept in narrow range from 3.75µH to 3.80µH. Table 3 shows the output voltage (V_{OUT}), current through the power supply (I_{DD}), output power (P_{OUT}), DC supply power (P_{DD}), and the efficiency (η) for each value of LA.

TABLE III
EFFICIENCY REGARDING LA

LA [H]	V_{OUT} [V]	I_{DD} [A]	P_{OUT} [W]	P_{DD} [W]	η [%]
3.75µ	73.0	2.87	53.29	68.88	77.00
3.76µ	72.5	2.80	52.56	67.20	78.20
3.77µ	72.0	2.74	51.84	65.76	78.80
3.78µ	71.5	2.66	51.12	63.84	80.07
3.79µ	71.0	2.58	50.41	61.92	81.41
3.80µ	70.0	2.51	49.00	60.24	81.30

As we can see, output power (P_{OUT}= 53.29W) is the highest for LA=3.75µH. However, it is obvious that better efficiency can be obtained for lower but still sufficient output power. Using LA=3.79µH provides maximum efficiency of 81.41 % with P_{OUT}=50.41W which is just above the specified minimum of 50W. The efficiency is lower than theoretical because the predefined impedance of actuator and the operating frequency do not make room for better optimisation.

With the adopted vales for C, Ls and LA it should be checked how sensitive the design is to parameter tolerances. Therefore three Monte Carlo analyses have been performed.

The first was for C1=C2=56pH, L3=L5=5uH (L4=2L3, L6=2L5) with 10% tolerances. It exhibited almost no effect on output voltage. Precisely, its magnitude varied between 69V and 71V.

The second took into account both output transformers. All four inductances have been adopted with 10% tolerances independently. This means that transformation ratio have been included as well as mismatching effects on output loads for M1 and M2. Fig. 9 presents the obtained results.

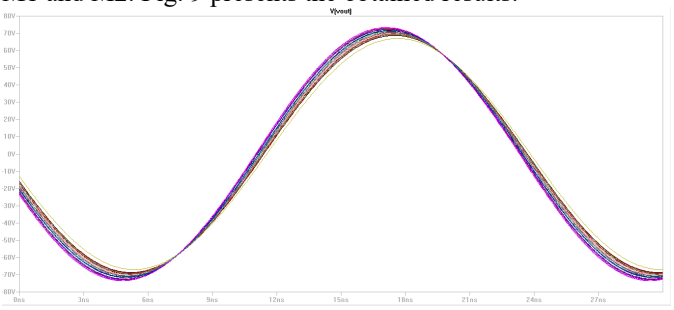

Fig. 9. Results of Monte Carlo analysis obtained for L_3=5µH ±10%, L_4=10µH ±10%, L_5=5µH ±10%, L_6=10µH ±10%

Obviously both the transformer rations and their mismatch affect the decrease of output voltage for less than 10% (the worst case magnitude was >65V).

The third Monte Carlo analysis has been repeated when LA and CA changes with tolerances 10%. The results are illustrated in Fig. 10. They indicate that 10% tolerances of the resonant circuit (LA and CA) parameters significantly affect the output. This was expected due to the high selectivity of serial resonant circuit. Consequently, in order to optimise circuit performance it is very important to match LA and CA

for the resonant frequency. It is good to know that during the welding process CA changes the value as the plates of the actuators comes closely when plastics begin to melt. Therefore it is important to provide LA that fits to resonance frequency with the initial value of CA at the beginning of the process.

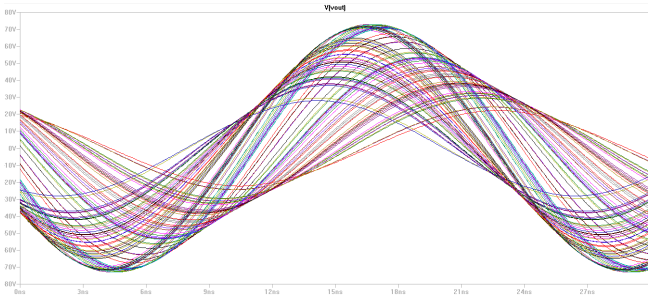

Fig.10. Results of Monte Carlo analysis obtained for C_A and L_A with 10% tolerances.

VI. CONCLUSION

This paper represents an extension of previously published paper explaining power RF generator design [2]. Practically the generator is aimed to provide sufficient power needed for RF welding of plastic tubes that are used in medicine. Namely bodily liquids are stored in plastic bags that end with plastic tubes. The RF welding is needed to seal the tubes quickly and reliably and to keep the liquid from contamination and leakage. The design is constrained with quantified requests enforced by physical phenomena during the welding process. Therefore, the required output power is 50W at 50Ω load. Besides, standards that regulate usage of radio frequency bands allow operating frequency of 40.68 MHz for medical appliances. The generator is loaded with an actuator that performs the welding by applying high electrical RF field on plastic material settled between two metal plates. Due to the friction between particles within the plastics it starts to heat until reaches melting temperature. Therefore the required power should be generated on an imperfect capacitor with loses. The most efficient way to increase the field is to connect the capacitor in series with an inductor and to fit for resonance frequency. Therefore the output stage of RF generator is loaded with serial resonance circuit.

Addition design requirement was high efficiency. Therefore RF power amplifiers that operate in Class E were considered for the output stage. Firstly, the simplest single transistor configuration has been considered. It provided very good efficiency of 83 %, but the output power has been less than 10W that is below the required 50W.

The output power has been increased utilizing a transformer with 1:3 transformation ratio. This has raised the output power to 45W but decreased efficiency to 73%.

The further improvement in trading power for efficiency provided solution with two transistors operating in push-pull configuration. The results obtained with the manually calculated circuit parameters provided output power of 50,46W with efficiency of 81,09%. The power increase is the result of adding the signal at the output transformer.

In order to find the maximum efficiency, parametric analyses have been performed on:

- capacitances C1=C2,
- inductances L4 = L6 that define the transformation ratio of output transformers (L3, L4) and (L5, L6), and
- inductance LA.

These resulted with slightly improvement of efficiency to 81,41% with small decrease of output power to 50.41W.

Finally, it is important to stress that operating at given resonance frequency using capacitor with predefined dimensions and dielectric properties give very limited space for parameter fitting. Moreover, Monte Carlo analyses showed that circuit is very sensitive to circuit parameters in output serial resonant circuit. It is expected that RF generator be practically implemented and therefore it should be upgraded and optimized for robustness in the future.

ACKNOWLEDGEMENT

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Response Distribution Analysis for Oscillator Circuit Due to Process Variation

Miljan Petrović and Miljana Milić

Abstract - In this paper we will try to analyse the influence of different statistical shapes and features of the technology parameters distributions to component behaviour, and consequently to the circuit response distribution. In this way it will be possible to create the methodology that will widen the use of Monte Carlo analysis and make it applicable not only to process variation research, but also to modelling effects of IC component aging, yield estimation, etc. The procedure will be demonstrated on the simple oscillator circuit through accessing process variation features of 555 timer component, and is based on multiple LTspice simulations, and statistical tools of the Matlab programme.

Keywords – MC analysis, Process variations, Tolerance, Response distribution, PDF.

I. Introduction

The process variation is one of the main factors examined in PVT (Process Voltage Temperature) design of analog circuits, that deals with numerous naturally occurring variations. Particularly, process variation represents changes of the semiconductors' attributes during IC fabrication process. It can cause significant and affective distortion in the output performance of analog circuits due to characteristics mismatch. These circuit response variations can be efficiently predicted in order to avoid the misspecification of a particular circuit or device, reducing the overall yield.

The device mismatch can be defined as a small random variation in parameters of identically designed devices, which occurs during the IC manufacturing process [1]. The basic approach used by designers is increasing the size of devices sensitive to mismatch. This decreases relative error in the desired characteristic minimizing the mismatch. However, smaller devices and complex circuits require large scale Monte Carlo (MC) simulations in order to investigate the way individual mismatches affect the circuit in whole. Hence, it is of great importance to correctly set up and perform simulations.

In the field of process variation, two directions of research have been emerged. Exploring the effects of process variation is often necessary for studying the influence of age to component performance [2], [3], [4]. Second, and equally important application of the analysis result is in the circuit design process, where designers have to build a circuit which is insensitive to parameters' fluctuations due to process variation [5], [6], [7], [1]. Special attention should be paid to the research described in [7], where the use of MC analysis is avoided, which is rare in literature and opposite to other references dealing with this problem.

Statistical Analysis implies running tens to thousands of simulations so that designer can analyze the behaviour of the circuit in accordance to variations of the active components' manufacturing process. Process variation data for a certain component are usually provided by the manufacturer and obtained through systematic testing and measurements. The results of such measurements are being mapped to corresponding model files. However, this procedure can be far more consuming in time and resources for complex IC components. One of the goals of this paper is to stress out the possibility and efficiency of using a simulation based method, rather than the mentioned procedure, for accessing process variation features of the IC.

The aim of this study was to examine process variation features of a complex semiconductor component encompassed in an analog circuit. By performing detailed statistical analysis of the simulation results, effects of underlying distributions of component parameters on the circuit response are discussed. Also, an elaboration is given on the selection of measures of distribution of component parameters, in order to select the best fit for the particular purpose (process improvements, aging effects, testing of parametric defects, tolerance design, yield estimation, etc) [8].

In the following sections a demonstration of MC based statistical response distribution analysis shall be provided. A short description of the simple oscillator circuit and reasons for choosing it as a subject of the analysis method will be given. Next, the methodology of the statistical analysis, based on Spice simulations and statistical Matlab [9] tools, will be explained in more detail. As the result, we have demonstrated the analysis for the response distribution of a simple oscillator circuit and gave the explanation and conclusions of the obtained statistical measures. Further research will be listed in the conclusions.

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II. The Oscillator Circuit

Response distribution analysis is performed on an oscillator circuit shown in Fig. 1. The element whose process variation data are being examined is the NE555 timer IC. The circuit is described in LTspice [10]. The subcircuit for the IC is the original Linear Technology copyrighted netlist NE555, with additional changes as explained in Section 3.

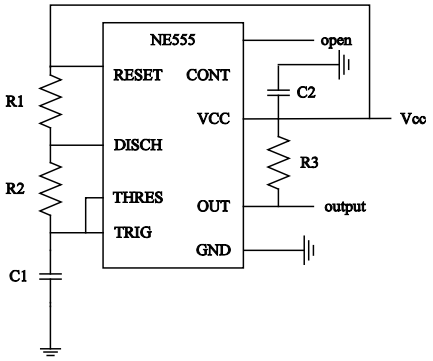

Fig. 1. NE555 based oscillator circuit

TABLE I
Values of Elements in Oscillator Circuit

Circuit element	Value
R_1	5 kΩ
R_2	3 kΩ
R_3	1 kΩ
C_1	0.15 μF
C_2	0.01 μF
V_{CC}	15 V

The oscillator is an astable multivibrator generating rectangular periodic output signal. This circuit appears suitable for response analysis, since it generates a single scalar output value, which, in fact, is the fundamental frequency of the output signal; the waveform itself is not relevant to the analysis. Since the behaviour of the circuit relies on charging the capacitor C_1 through resistors R_1 and R_2, and discharging through R_2, these are the elements that define the output frequency as in Eq. (1):

$$f \approx \frac{1.44}{(R_1 + 2R_2)C_1} \tag{1}$$

where f is the working frequency, and resistances R_1 and R_2 and capacitance C_1 are values of circuit elements according to Fig. 1. Values of all the elements for the designed oscillator are listed in Table I. The corresponding frequency should be 872.7273 Hz.

However, after Spice simulation was performed, it was observed that due to specific component modelling the working frequency is 928.79 Hz. This value is taken as nominal in regard of the latter statistical analysis.

III. Methodology of Statistical Analysis

The first step in analysis of the described circuit is performing MC simulations. Several groups of data are acquired. Namely, the output signal of the circuit is generated in LTspice for 1000 simulations per each set of parameters. These parameters are: the tolerance T of passive elements of the NE555 Spice model, and the type of the statistical distribution, from which the values of these elements are generated. Since the most common types of distributions used in MC analysis are uniform [5], [6] and Gaussian [1], they both are implemented for the purpose of this paper. In the case of Gaussian distribution, the tolerance T implies that the variance of the distribution is $\sigma^2=(T/100)^2$, where T is expressed in percents. The mean of the distribution is the nominal value of the Spice element which is the part of the original netlist. In the case of the uniform distribution, T is in fact the tolerance, i.e. maximal relative distance between the generated value and the center of the distribution. The circuit displayed in Fig. 1 is implemented in LTspice with commands for transient MC simulations. Formulae for random number generation according to the described distributions are also included in the Spice netlist. For different types of distributions, separate netlists are extracted. Namely, the generation of passive elements' values for timer model is defined by the type of underlying distribution. On the other hand, values of external elements of the oscillator circuit are fixed. These include resistances R_1, R_2 and R_3, capacitances C_1 and C_2 and DC supply voltage V_{CC}.

Finally, a thousand output signals with the duration of 50ms (approximately 46.5 periods of oscillation) are generated for two types of distributions and and three particular tolerance values: T=2%, T=5% and T=10%. Consequently, these results are imported in Matlab for further statistical processing. A script has been written in order to calculate the fundamental frequency and transform sets of output signals into sets of frequency values. The frequency is derived by calculating the discrete Fourier transform (using FFT algorithm) and finding the location of the maximal amplitude component in the spectrum. In order to achieve good accuracy, some additional HP filtering was implemented.

After all the frequencies are acquired, significant statistical quantities are calculated for each of 6 sets. Namely, several central moments are estimated, which, in compliance with [11], can be defined as in (2):

$$\mu_n = E[(X - E[X])^n] \tag{2}$$

where μ_n stands for n^{th} central moment, X denotes the random variable, E is the expectation operator ($E[X]$ is the

mean, i.e. the first moment of X), whereas n can have values 2, 3 and 4, respectively. Sample estimation is performed for the lowest four central moments, i.e. mean, variance, skewness and kurtosis. Used sample estimators are unbiased.

Empirical PDFs (probability density functions) were calculated next (histograms and kernel-smoothing density estimated functions), and compared to known mathematical distributions. Different information criteria was used to fit numerous distributions to generated data, and each gave the best fit with its minimal value. The used criteria are: Bayesian Information Criterion (BIC), Akaike Information Criterion (AIC), Akaike Information Criterion with correction for finite sample sizes (AICc), and negative log likelihood (NLogL). The implemented algorithm results in different best fits for cases of Gaussian and uniform element values distribution.

IV. Analysis Results

Tables II and III contain unbiased estimates of the four lowest central moments of the response distribution. Table II considers the Gaussian random generation, whereas Table III considers the uniform. The simulation of the nominal NE555 model gives the frequency of 928.79Hz. However, results from Table III show the relative error of the frequency mean is around 2% for all tolerances (the estimated mean is between 910Hz and 911Hz). It can be noticed that the estimated mean increases with the tolerance when Gaussian generation is used. According to the chosen underlying distribution for passive elements, it is clear that in general, means and variance estimates are greater in Table II than in Table III. It can be concluded that Gaussian MC analysis represent the worse one in comparison to the uniform MC.

TABLE II
Estimation of Moments of Response Distribution Under Gaussian Distribution for Passive Elements Generation

tolerance / moment order	T=2%	T=5%	T=10%
1 (mean)	911.272387	913.097827	920.208811
2 (variance)	610.489362	3643.53864	15206.2522
3 (skewness)	0.04797167	0.17813189	0.46685908
4 (kurtosis)	3.04642211	2.88281022	3.07880775

TABLE III
Estimation of Moments of Response Distribution Under Uniform Distribution for Passive Elements Generation

tolerance / moment order	T=2%	T=5%	T=10%
1 (mean)	910.936195	910.633842	910.840261
2 (variance)	134.645217	587.226402	2269.23186
3 (skewness)	-0.2468981	0.06193966	0.11390945
4 (kurtosis)	3.14433509	2.57091046	2.46468484

Data in Tables II and III correspond to Figs. 2 and 3 where kernel-smoothing PDF estimates of each set of frequencies is plotted. Conclusions derived from results of mean and variance are illustrated in these plots. Also, skewness and kurtosis are sometimes easier to examine visually. Namely, uniform based data show response distributions oriented more to the left, and Gaussian base to the right, which is confirmed both with plots and skewness estimates. However, skewness analysis only makes sense for unimodal distributions. It is also interesting that at lower tolerances T, response distributions tend to be multimodal and their PDFs show several local extremals, which is observable in Figs. 2 and 3.

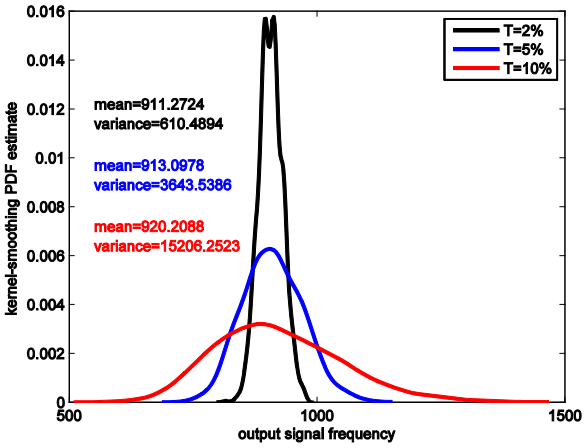

Fig. 2. Kernel-smoothing PDF estimate for tolerance values of 2%, 5% and 10% in the case of Gaussian distribution based generation of passive model elements

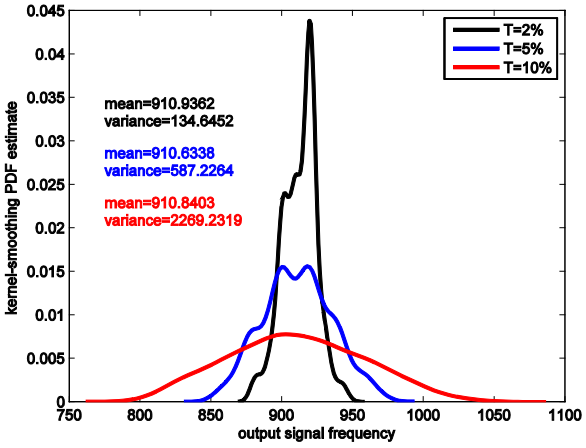

Fig. 3. Kernel-smoothing PDF estimate for tolerance values of 2%, 5% and 10% in the case of uniform distribution based generation of passive model elements

After estimation of central moments, the best fit for response distributions should be determined next. For each

set of frequencies information criteria are calculated in order to check if the data comes from certain distributions. The investigated distributions are: generalized extreme value, Birnbaum-Saunders, inverse Gaussian, log-normal, gamma, Nakagami, Rician, normal (Gaussian), t location-scale, log-logistic, logistic, Weibull, extreme value, Rayleigh and exponential distributions [11], [12]. The calculated criteria for sorting the fits were: NLogL, AIC, AICc and BIC. Examples of fitting can be seen in Figs. 4 and 5. Fig. 4 shows normalized histogram (empirical PDF) and two best continuous PDF fits (generalized extreme value and inverse Gaussian), according to AIC, in the case of Gaussian generation and T=10%. Fig. 5 shows normalized histogram (empirical PDF) and two best continuous PDF fits (generalized extreme value and Birnbaum-Saunders), according to AIC, in the case of uniform generation and T=10%. Plotting more fits at the same time makes the figure unclear since PDFs differ slightly.

The results of the best fits for each set of data and each criterion are listed in Table IV. The letter G stands for the Gaussian based generation of passive elements, whereas the letter U stands for uniform one. Abbreviations are used for distributions names so that the table can be more legible. These are: Γ for gamma, GEV for generalized extreme value, BS for Birnbaum-Saunders, IG for inverse Gaussian, TLOC for t location-scale and R for Rician.

TABLE IV
BEST FIT RESPONSE DISTRIBUTIONS FOR EACH SET OF FREQUENCIES AND EACH CRITERION

criterion / dataset	NLogL	AIC	AICc	BIC
T=2%, G	Γ	Γ	Γ	Γ
T=5%, G	GEV	BS	BS	BS
T=10%, G	GEV	GEV	GEV	IG
T=2%, U	TLOC	R	R	R
T=5%, U	GEV	GEV	GEV	GEV
T=10%, U	GEV	GEV	GEV	GEV

Comparing the results for AIC and AICc leads to an observation that all the fits for these two criteria are the same. This confirms the fact that the sample size of 1000 taken in provided analysis in this paper is large enough to derive statistical conclusions.

Also, it is of great importance to look at results of AIC and BIC. Namely, these criteria are essentially different. AIC is asymptotically optimal in terms of average square error, whereas BIC has the consistency property (it converges to the true model for larger sample sizes) [13]. However, these differences can be negligible considering presented results. The only case in which the type of best fit distribution is different according to AIC and BIC is the case of T=10%, G. The compliance of AIC and BIC is particularly emphasized in the case of uniform based generation and lower tolerances.

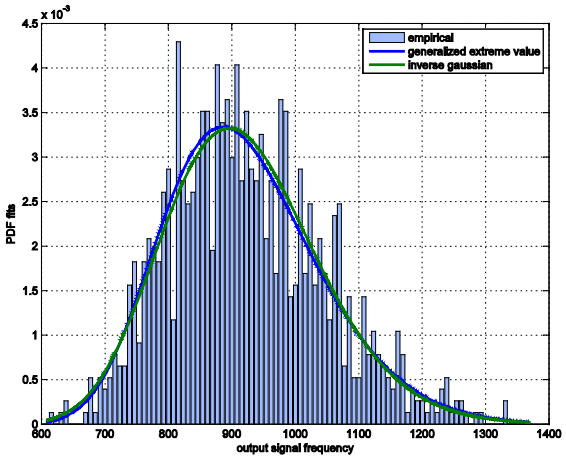

Fig. 4. Normalized histogram and two best fits for response distribution according to AIC at T=10% in the case of Gaussian distribution based generation of passive model elements

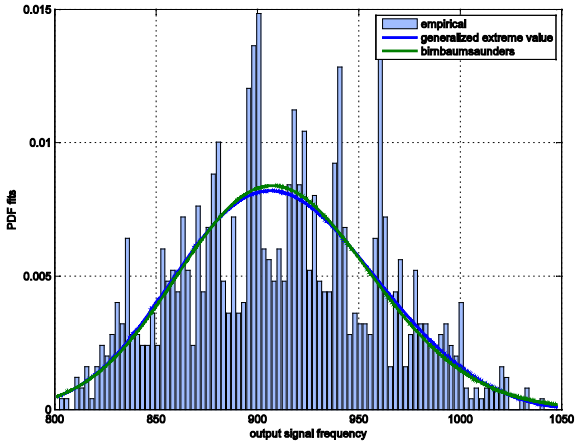

Fig. 5. Normalized histogram and two best fits for response distribution according to AIC at T=10% in the case of uniform distribution based generation of passive model elements

The best fits depend greatly on the value of tolerance T, especially in the case of Gaussian generation. However, generalized extreme value distribution is the most common best fit considering all cases. That is why GEV can be a reasonable assumption for response distribution under process variation of NE555, e.g. used in component aging analysis as in [2] and [4].

V. CONCLUSION

In this paper a methodology of MC based statistical analysis of an oscillator circuit has been described. Several significant conclusions were inferred through comprehensive examination of results. Those are referred to accessing process variation features of ICs. First, it was shown that, due to mapping of fabrication parameters to elements of the IC Spice model, effects of component's

process variation can be inspected by random generation of passive elements of the model during MC simulations and analysis of the response distribution. Further work can be focused on similar analysis including generation of other Spice model parameters beside passive elements' values. In addition, this paper provides an elaboration on the statistical process of generation in the sense of determining the proper type of distribution.

Agreement between results of best fits for response distribution calculated using different information criteria implies the acceptance of an assumption of component behaviour under process variation in further IC analysis. Namely, best fit for circuit response distribution can be used as assumed and analyzed component's process variation distribution. However, the correct determination of the assumption requires considering parameters of random number generation included in MC analysis.

Further research on the subject can be oriented towards the justification of proposed assumption in the process variation-aware aging analysis [2], [3], [4]. In this way, the analysis of these two equally important factors of system and component performance would be significantly facilitated.

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